

MODEL NAME : CAM00

PCB NO : LA-E331P

BOM P/N :

Dell/Compal Confidential

Schematic Document Berlinetta MLK (KABY LAKE-H)

2016-10-26

Rev: 1.0 (A00)

@ : Nopop Component

@SPAD@ : Nopop Component 0 Ohm Short-PAD

XDP@ : Nopop Component

CONN@ : Connector Component

R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB

TPM@ : TPM function

EMC@ : Pop of EMI parts

Q1VRAMS@ : Samsung GDDR5 for Q1-GPU

Q1VRAMM@ : Micron GDDR5 for Q1-GPU

G0VRAMS@ : Samsung GDDR5 for G0-GPU

G0VRAMM@ : Micron GDDR5 for G0-GPU

G0VRAMH@ : Hynix GDDR5 for G0-GPU

BreakDown@ : for measure power consumption

Q1@ : GPU N16PQ1 & N17PQ1

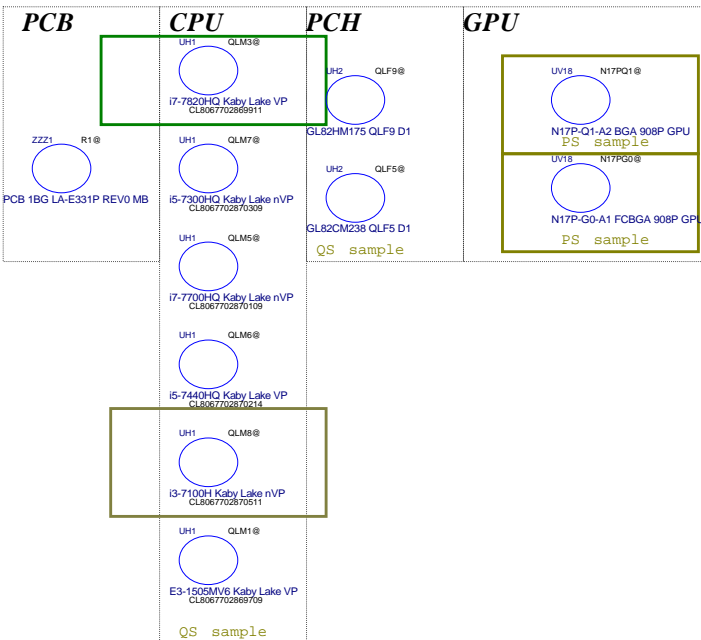
G0@ : GPU N17PG0

UMA@ / DIS@ : UMA/DIS

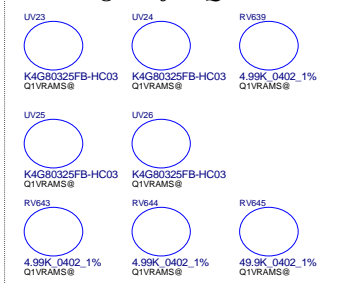
CSMB@ : G0

BC@ : Q1

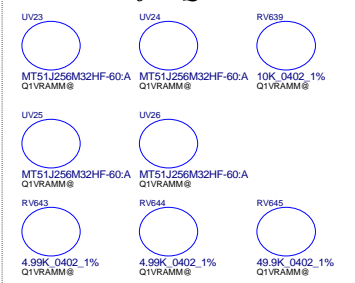
SPAD@ : Nopop Component 0 Ohm Short-PAD for NPI test require



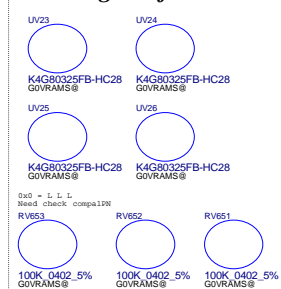
Samsung 8G for Q1



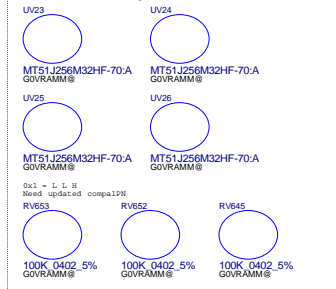
Micron 8G for Q1



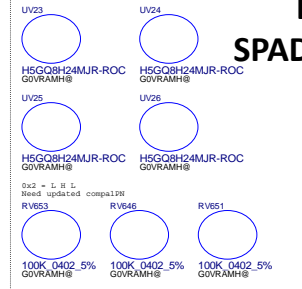
Samsung 8G for G0



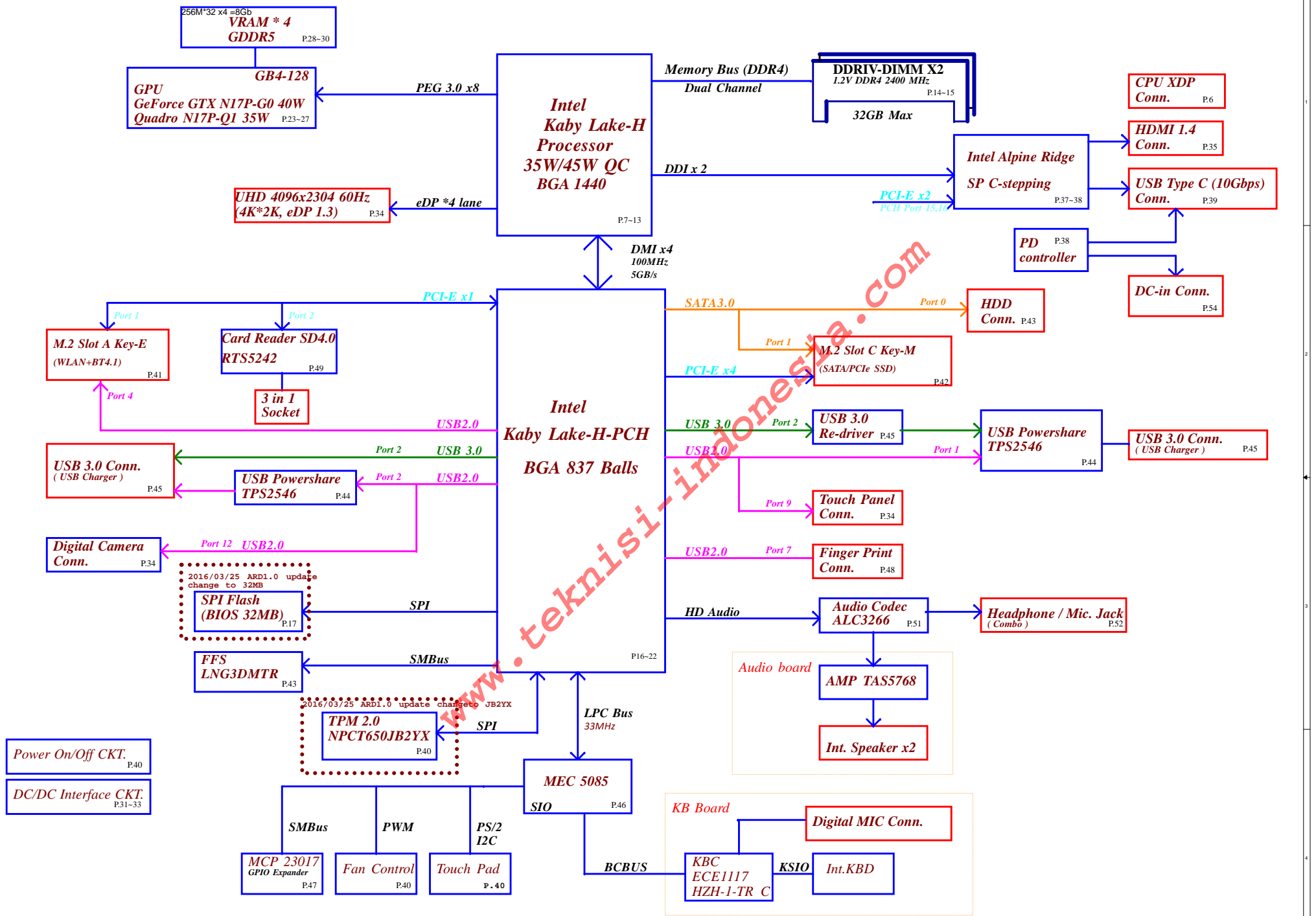
Micron 8G for G0



Hynix 8G for G0

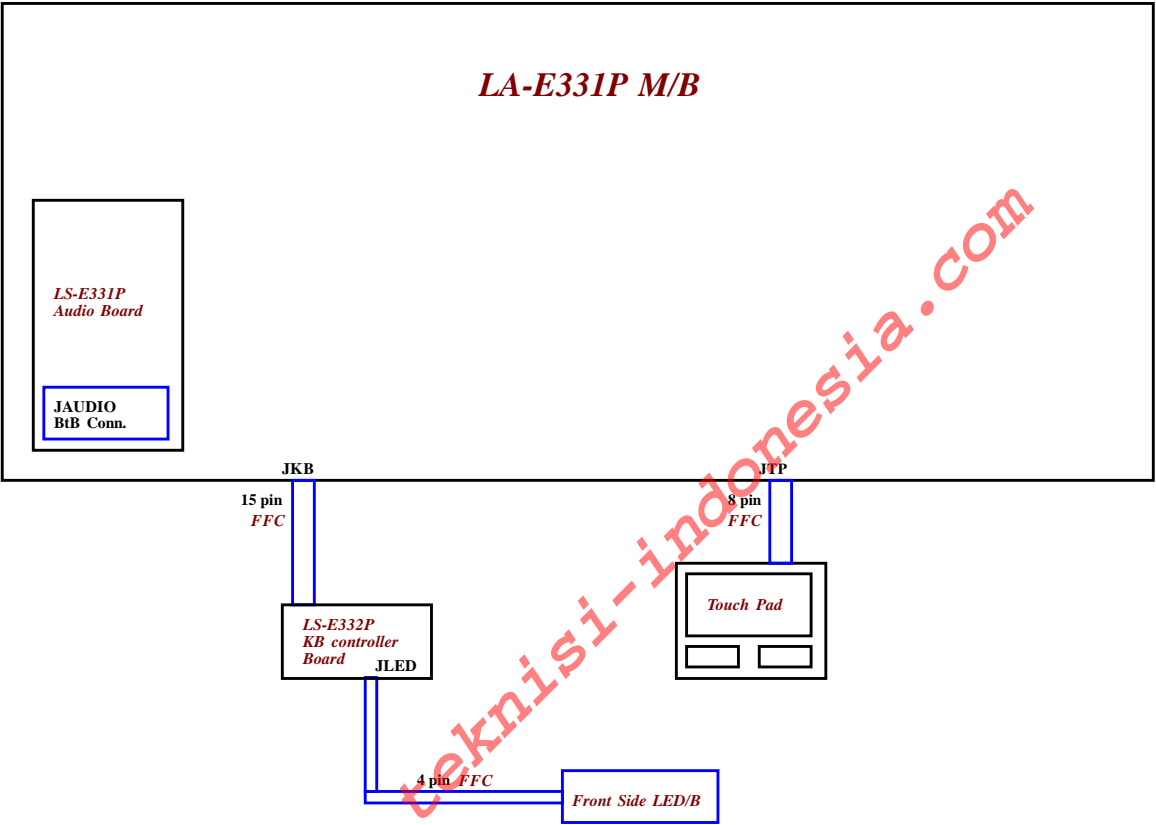


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				Size Document Number
				LA-E331P
				Date: Wednesday, October 26, 2016 Sheet 1 of 75



Compal Confidential

Project Code : CAM00
File Name :



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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title DB block diagram		
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Board ID	Resistor
X00	N/A
X01	
X02	
X03	
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA



DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

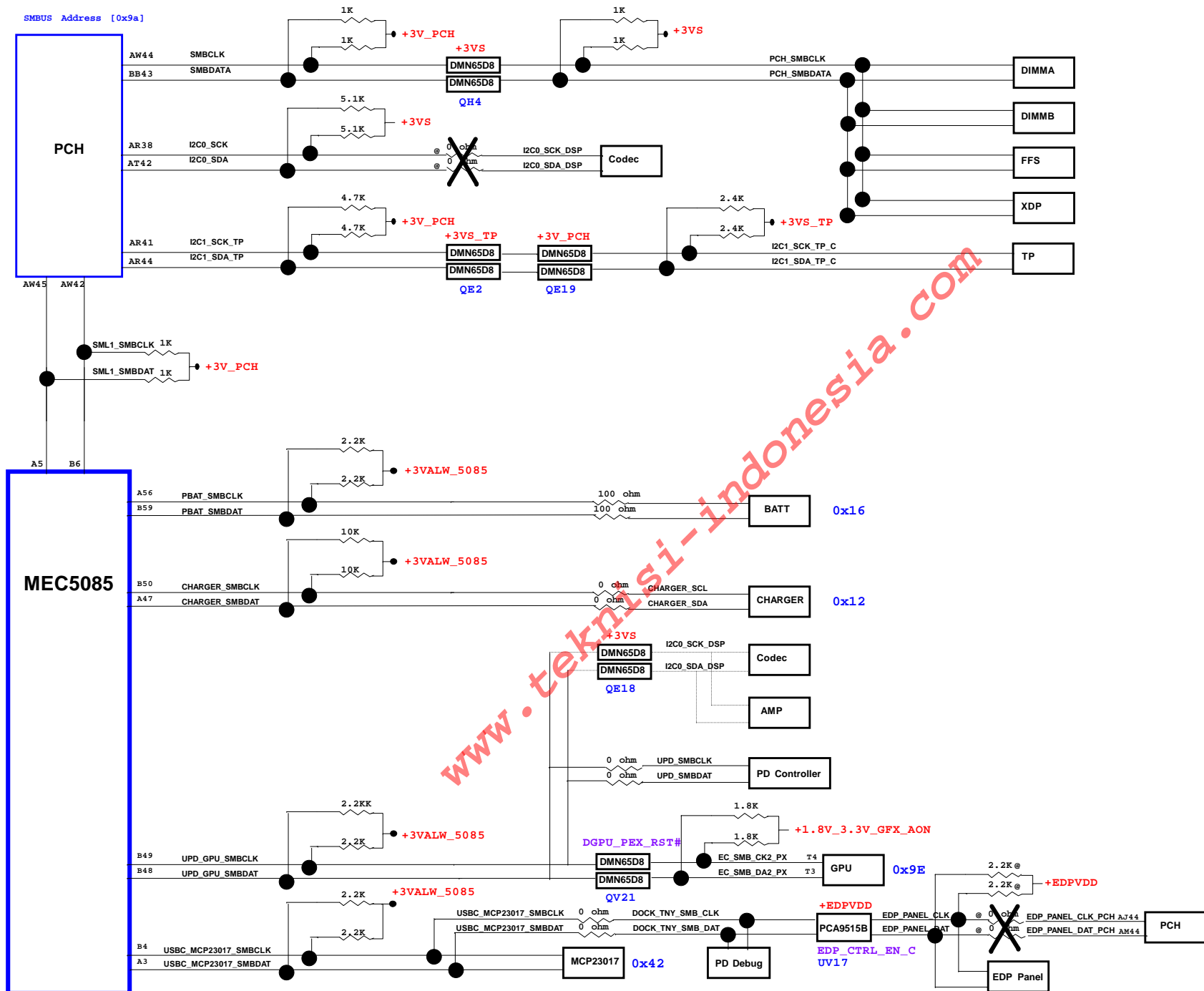
PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	CARD READER	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD	SATA	DESTINATION
Lane 10	SSD	0A	SSD
Lane 11	SSD	1A	N/A
Lane 12	SSD	N/A	N/A
Lane 13	SSD	N/A	N/A
Lane 14	SSD	0B	None
Lane 15	SSD	1B	HDD
Lane 16	SSD	2	None
	Alpine Ridge	3	None

LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

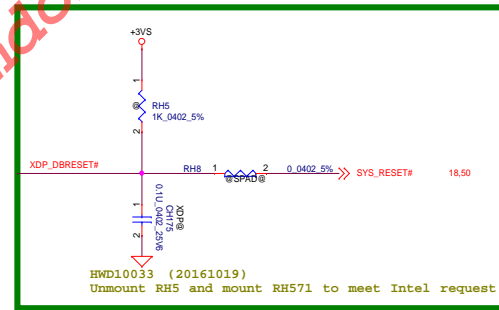
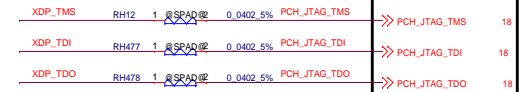
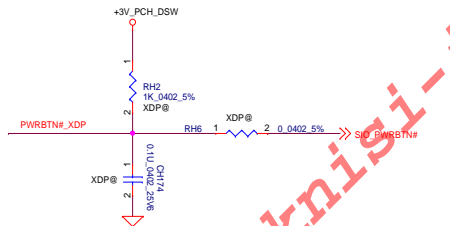
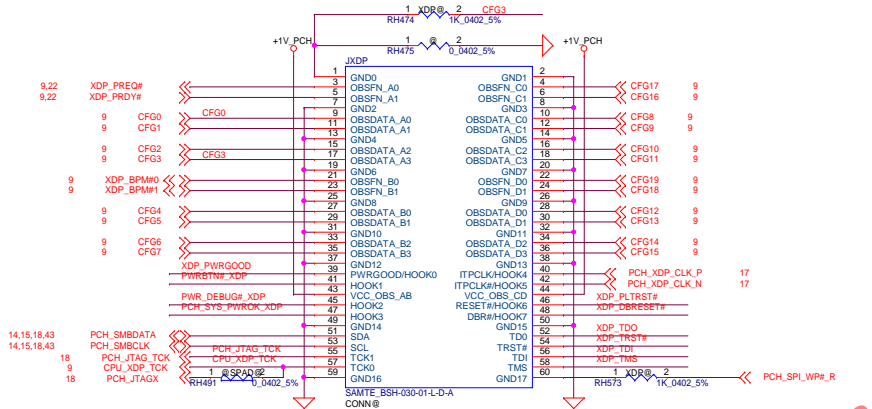
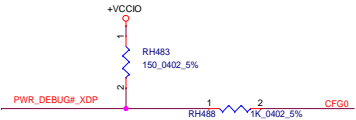
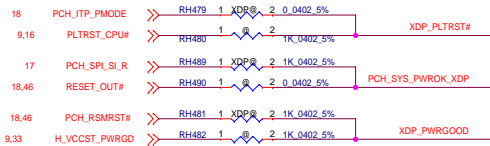
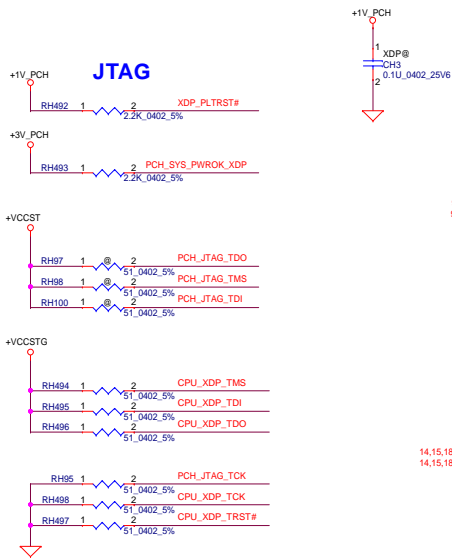
CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	None	13	None
4	NGFF-1 WLAN	14	None
5	CARD READER	15	None
6	Thunderbolt		
7	NGFF-2 SSD		
8	GPU		
9	None		

Symbol Note :

 : means Digital Ground
  : means Analog Ground

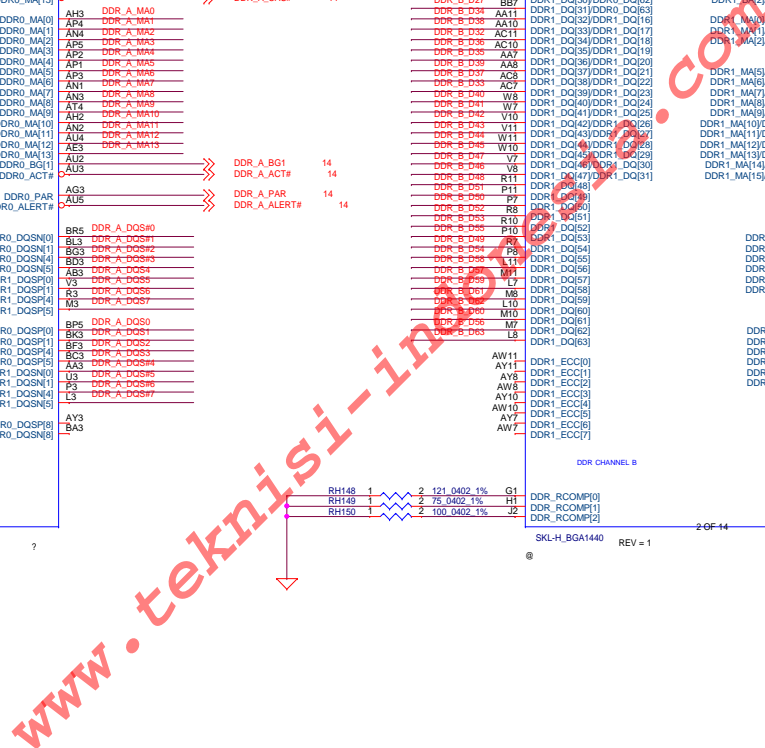


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Size		Document Number		Rev	
Custom				0.1000	
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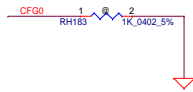
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Size	Document Number	Sheet	6 of 75	Rev 0.1(200)
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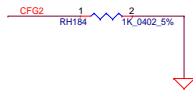
Date: Wednesday, October 26, 2016 Sheet 8 of 75

CFG Straps for Processor

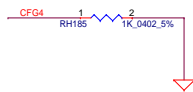
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	<p>* 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



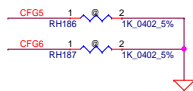
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>* 0: Lane Reversed</p>



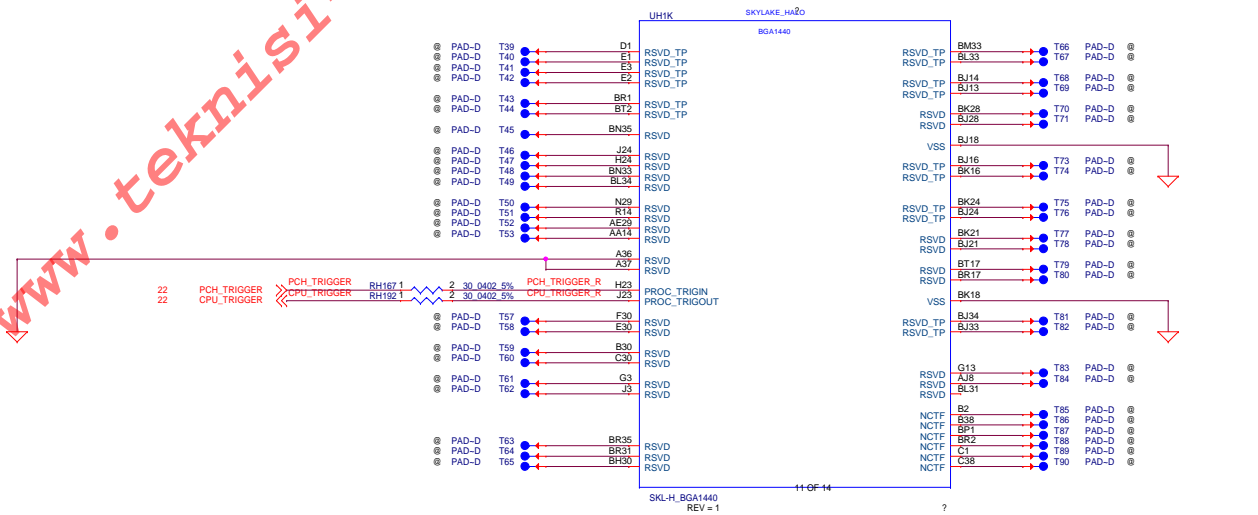
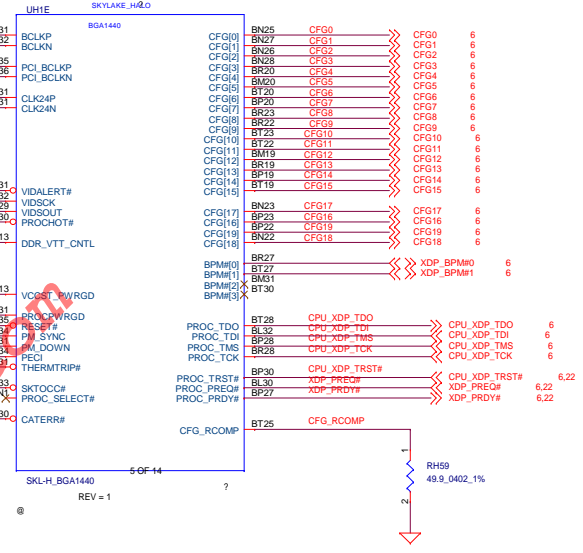
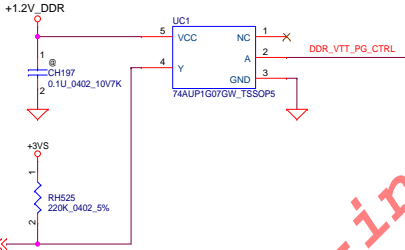
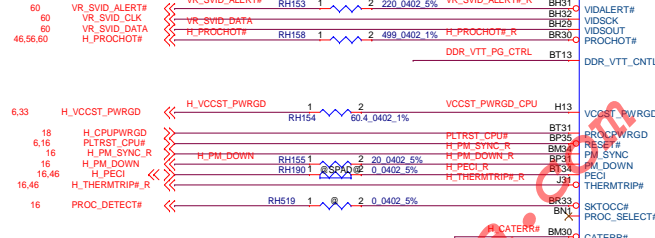
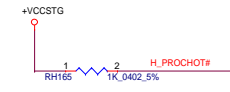
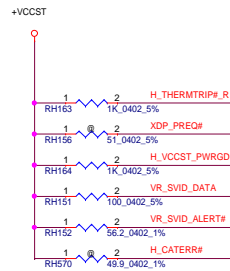
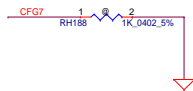
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

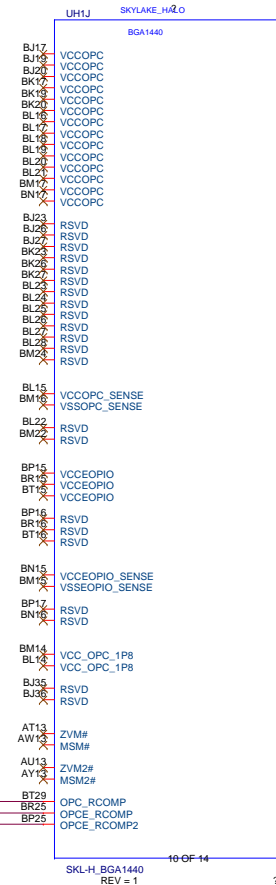
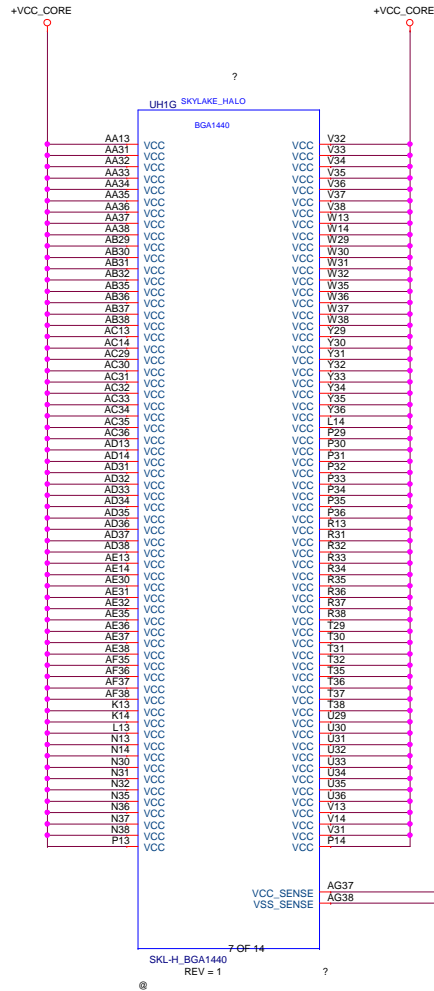


PCIe Port Bifurcation Straps	
CFG[6:5]	<p>* 11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>



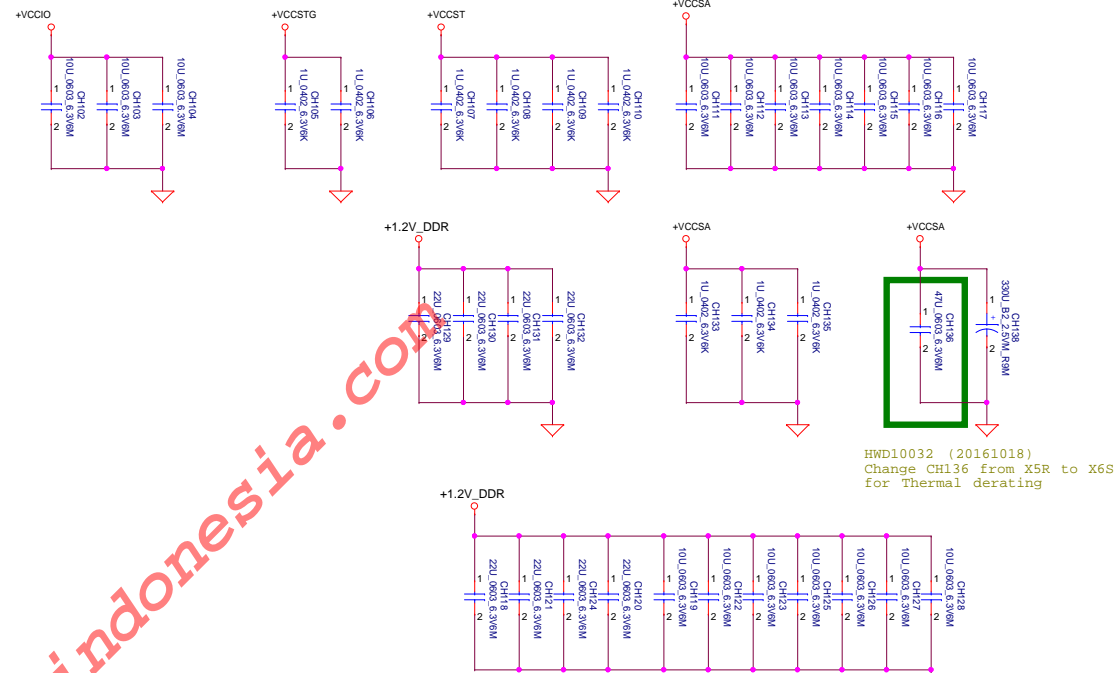
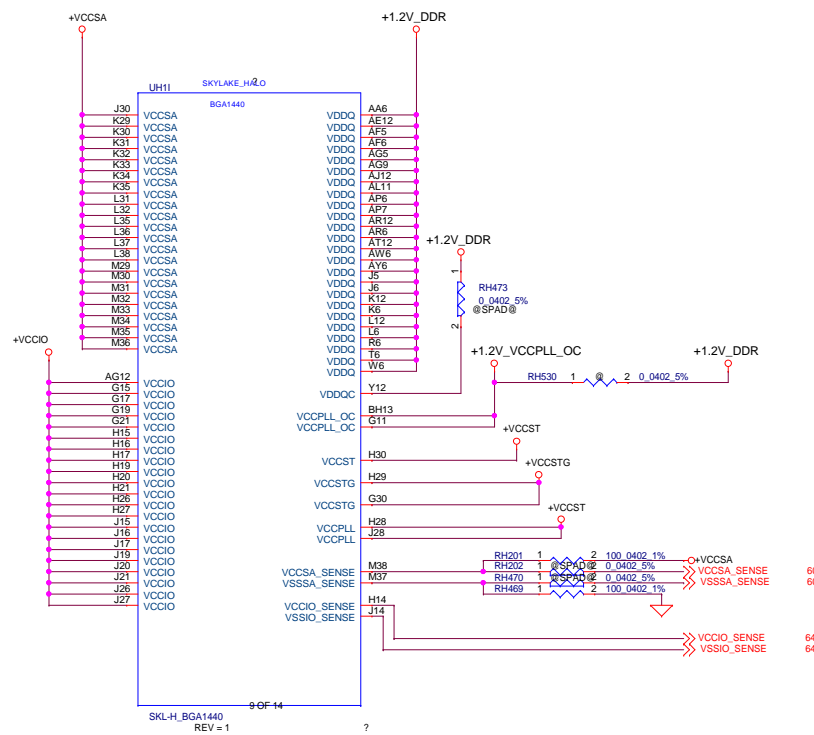
PEG DEFER TRAINING	
CFG7	<p>* 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>





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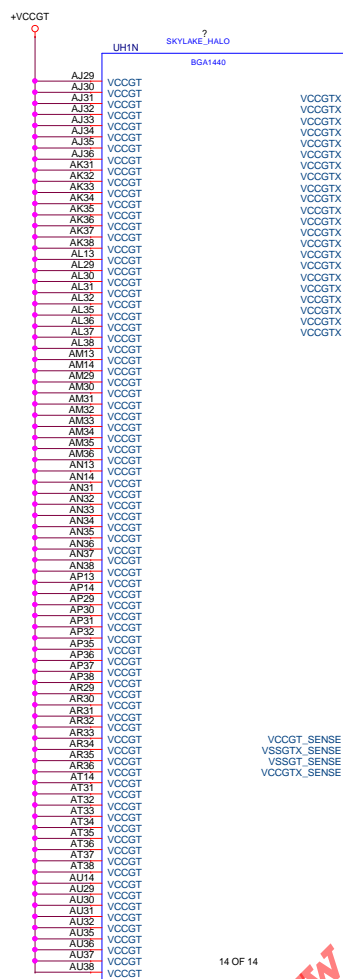
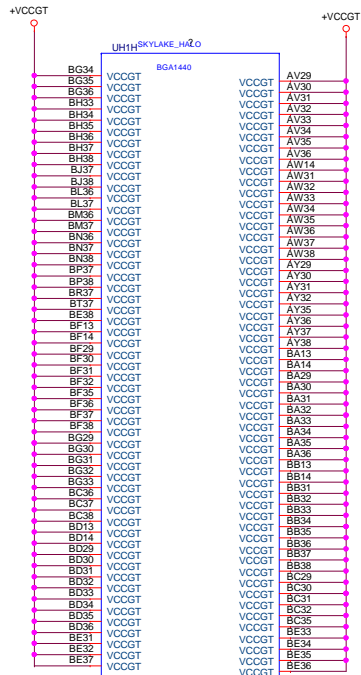
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HWD10032 (20161018)
Change CH136 from X5R to X6S
for Thermal derating

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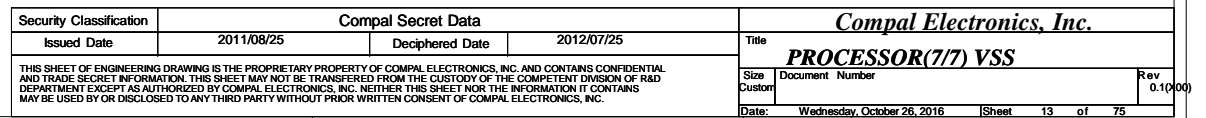
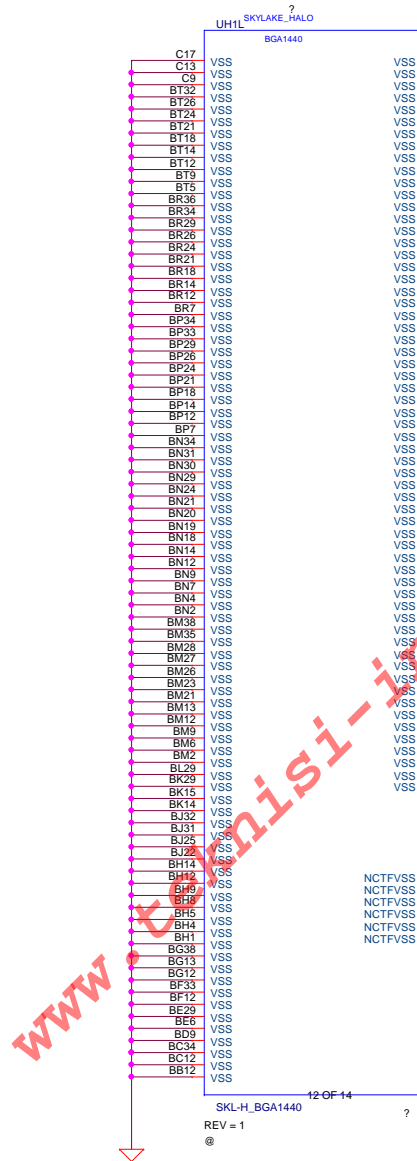
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Date:	Wednesday, October 26, 2016	Sheet	11 of 75	Rev	0.10000



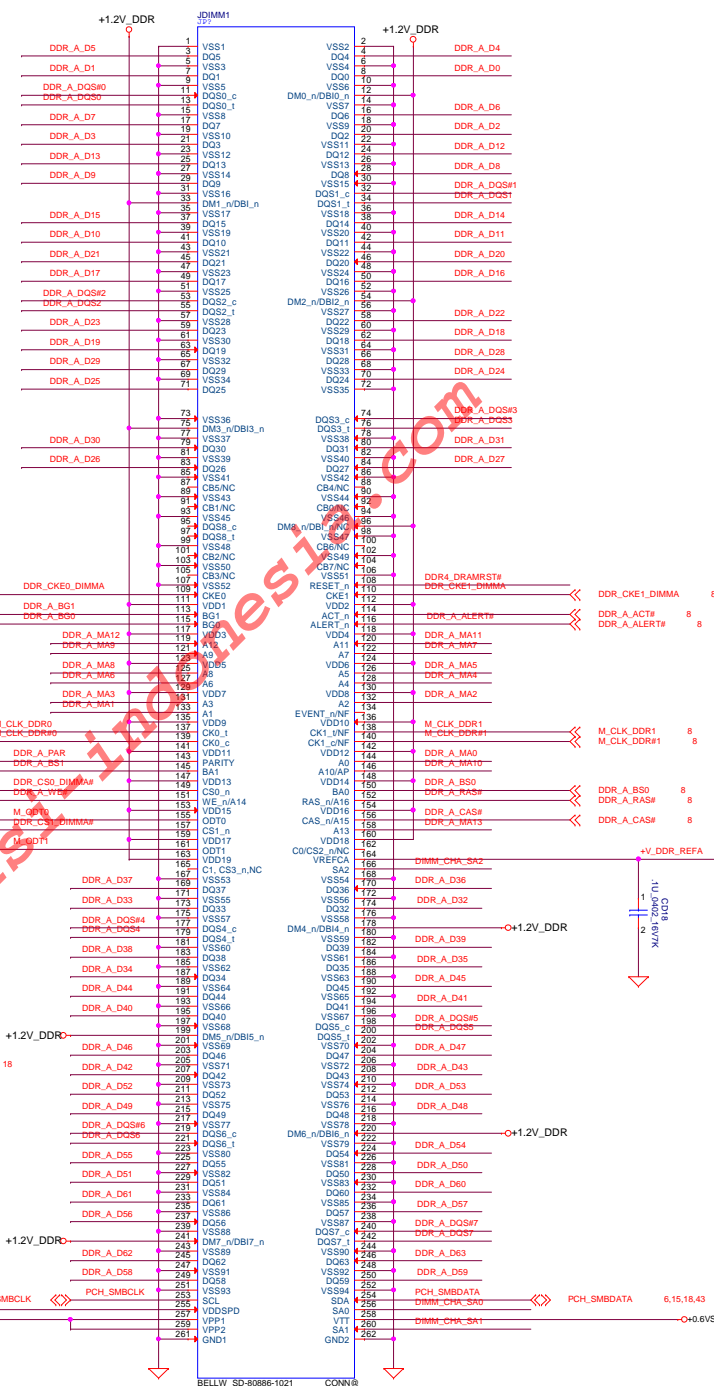
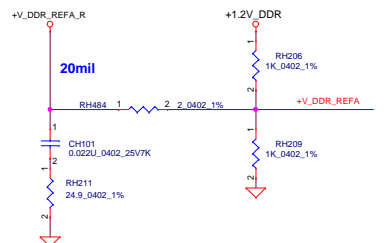
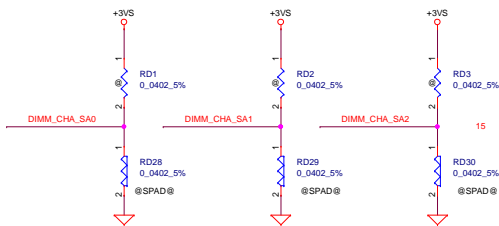
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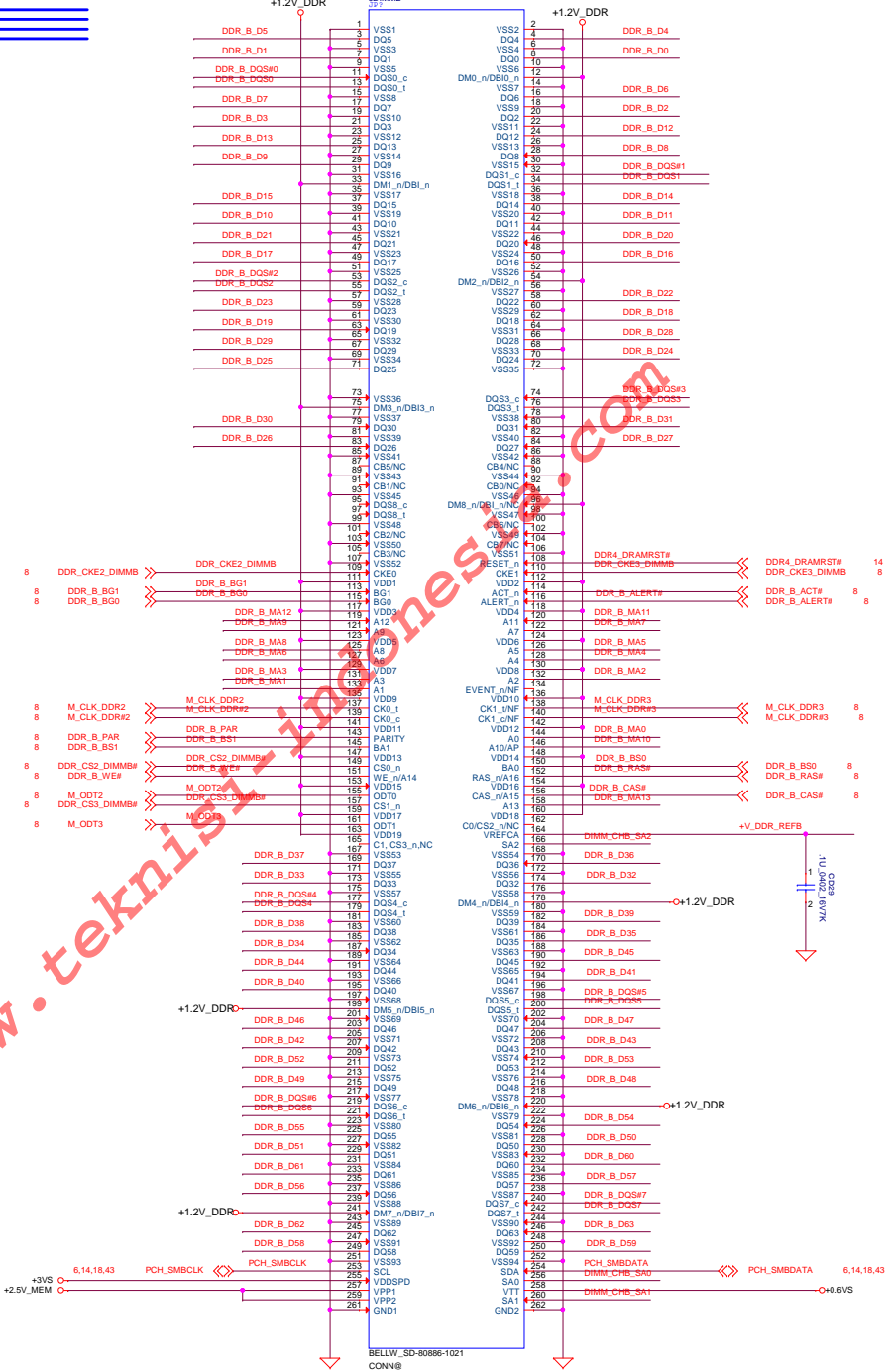
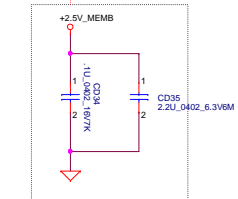
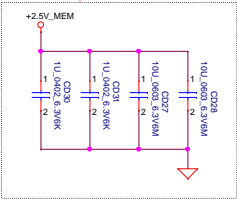
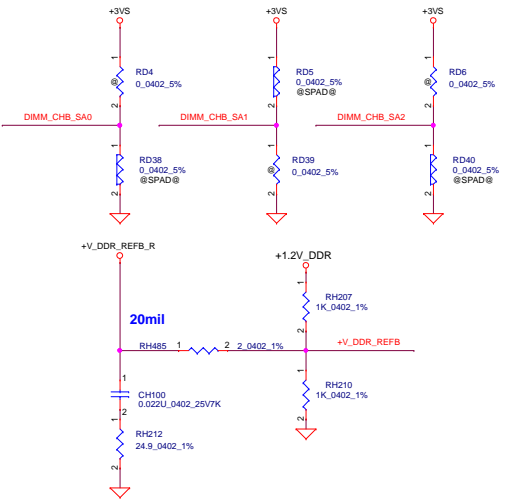


The circuit diagram shows a 5-bit DAC. It consists of a +0.6V source connected to a series of five capacitors, labeled CD12 through CD15. Each capacitor has a value of 1u, 0.603, 0.376V. The capacitors are connected in parallel to a common output line, which is connected to a ground symbol.



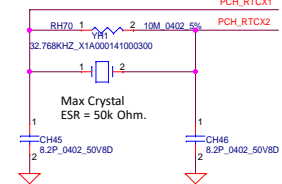
All VREF traces should
have 10 mil trace width

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All VREF traces should
have 10 mil trace width

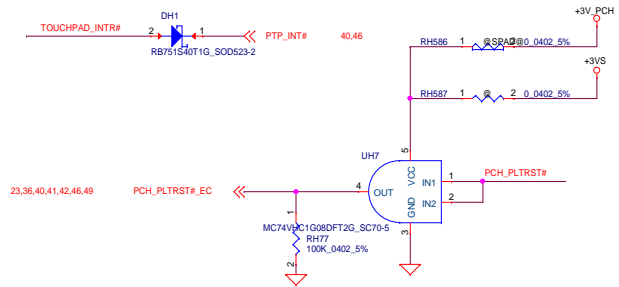
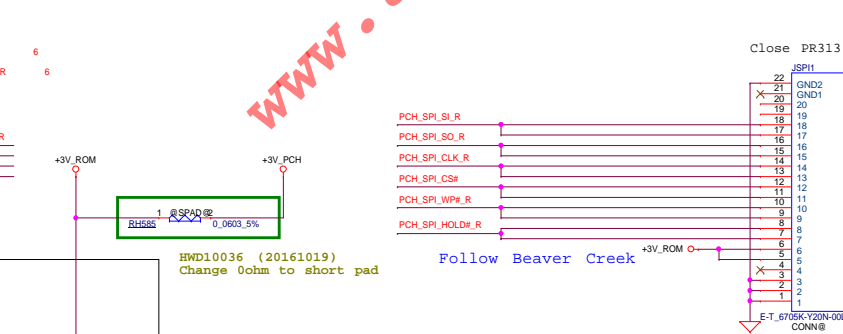
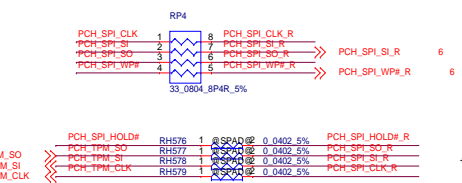
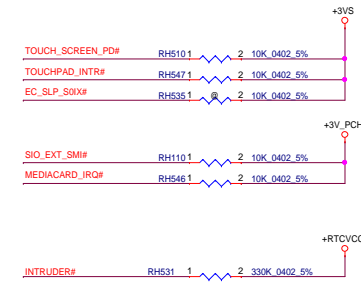
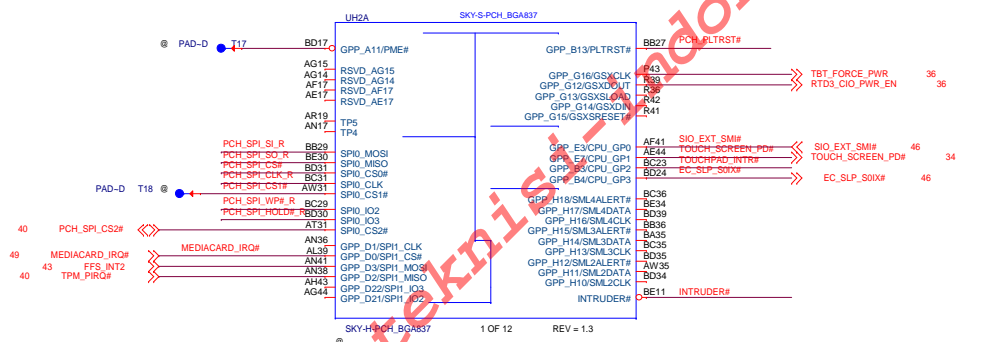
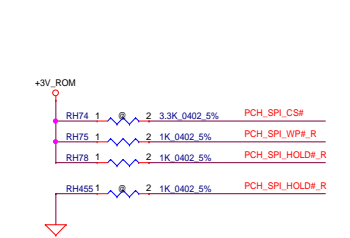
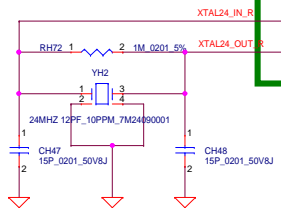
RTC CRYSTAL



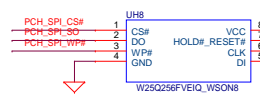
EMI10005 (20161003)
Change RA96/RA97 from 0 ohm
to 33 ohm for panel flicker issue

RA96 1  2 33 0201 5% XTAL24_IN

RA97 1  2 33 0201 5% XTAL24_OUT

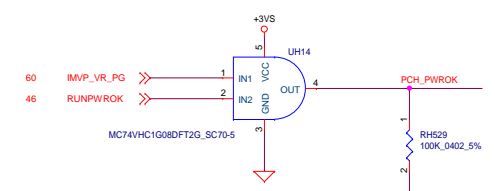
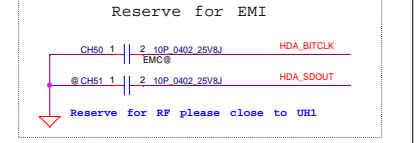
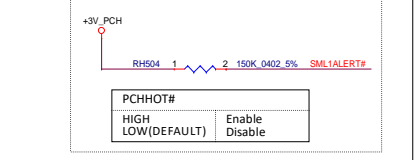
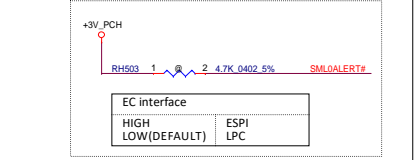
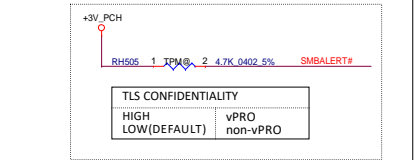
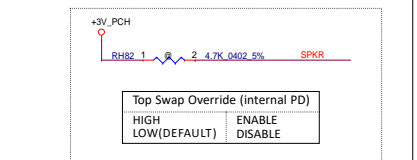
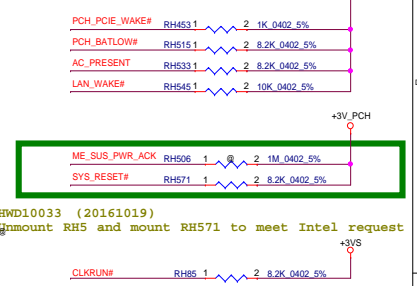
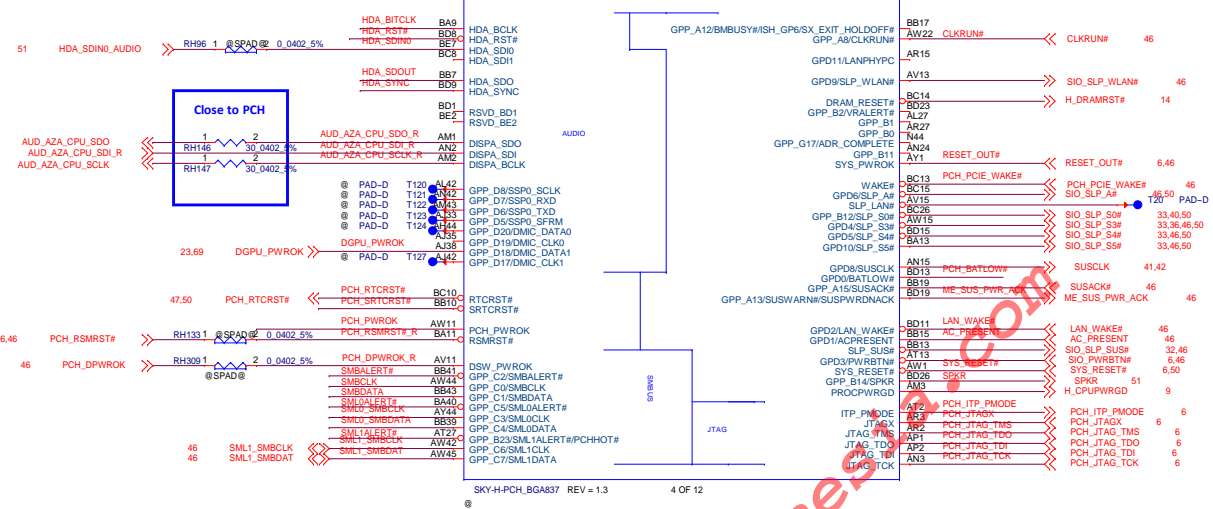
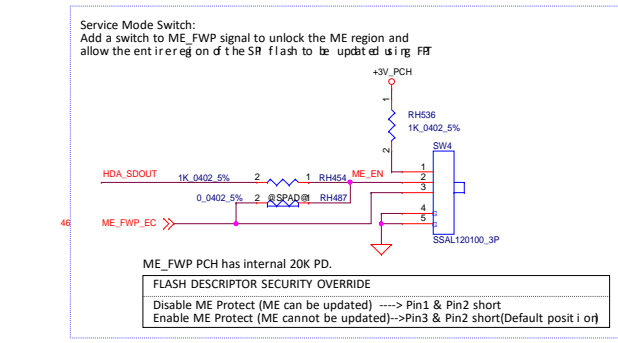
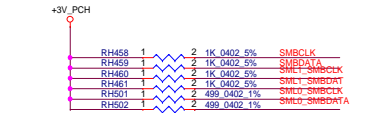
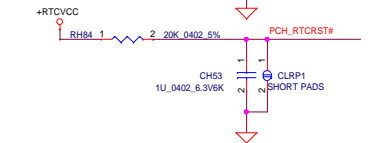
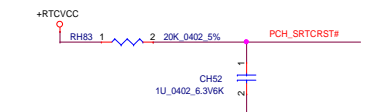
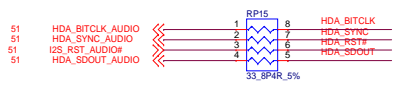


SPI ROM FOR ME (32MByte)

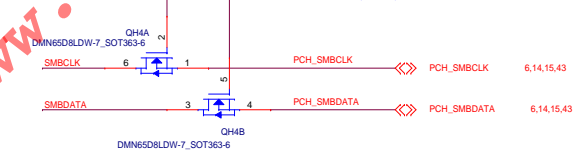


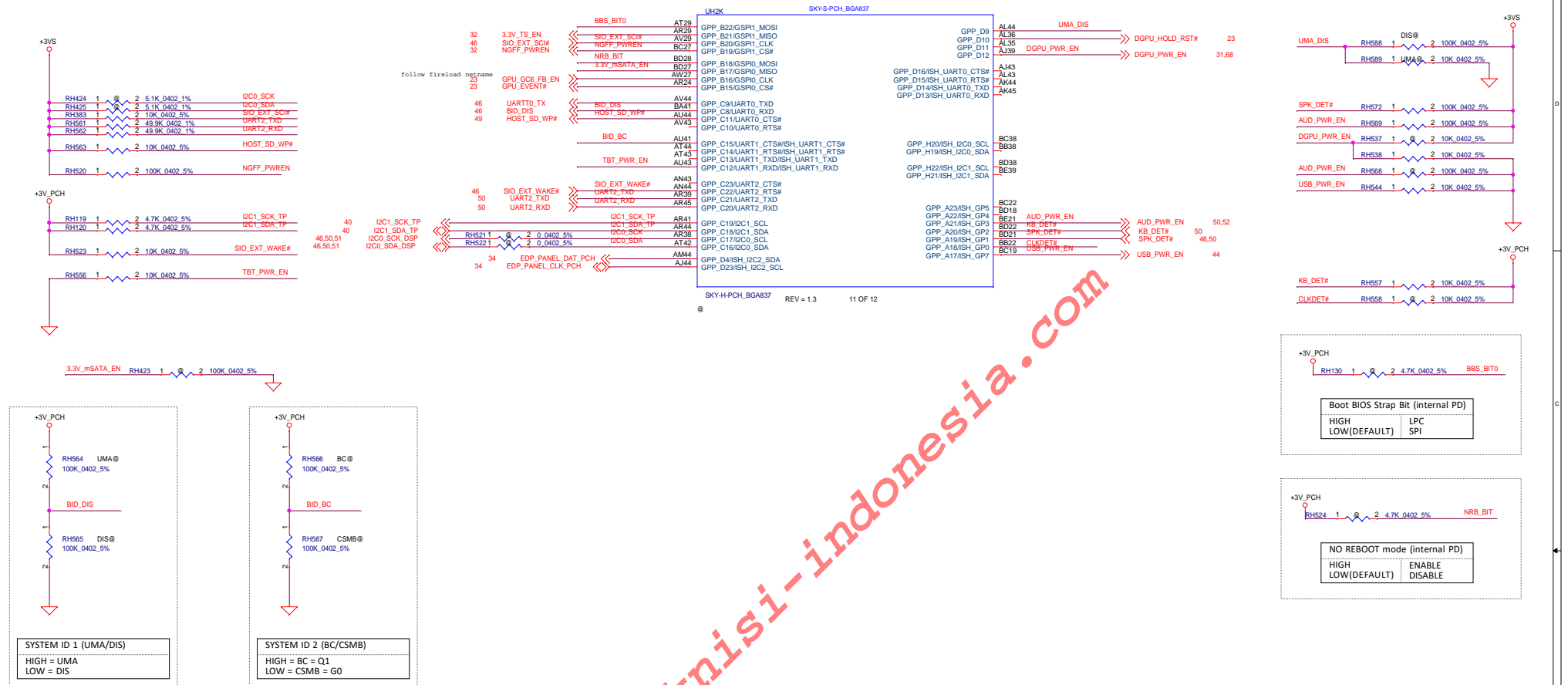
HWD10036 (20161019)
Change 0ohm to short pad

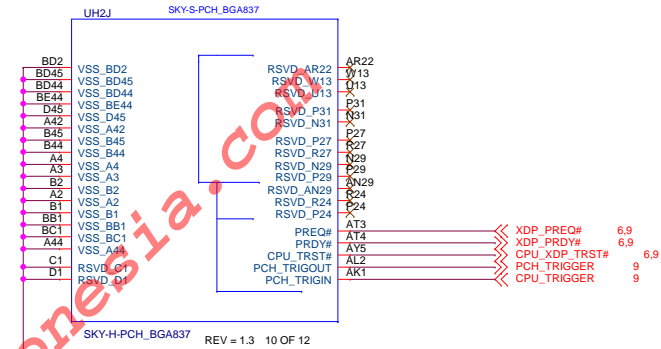
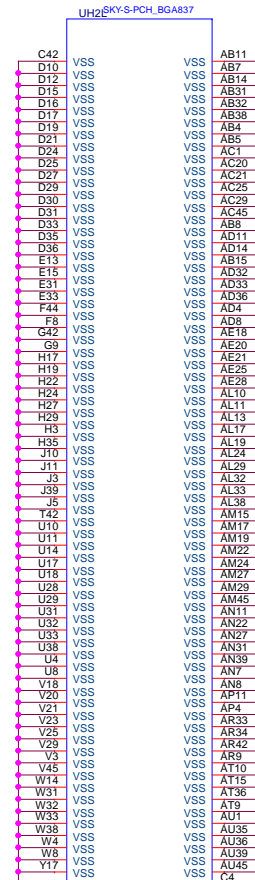
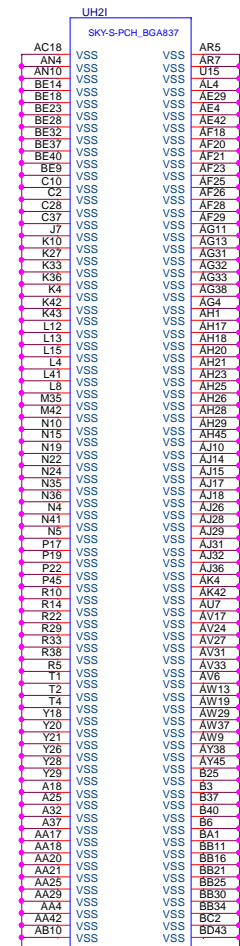
Follow Beaver Creek



PCH to DDR, XDP, FFS

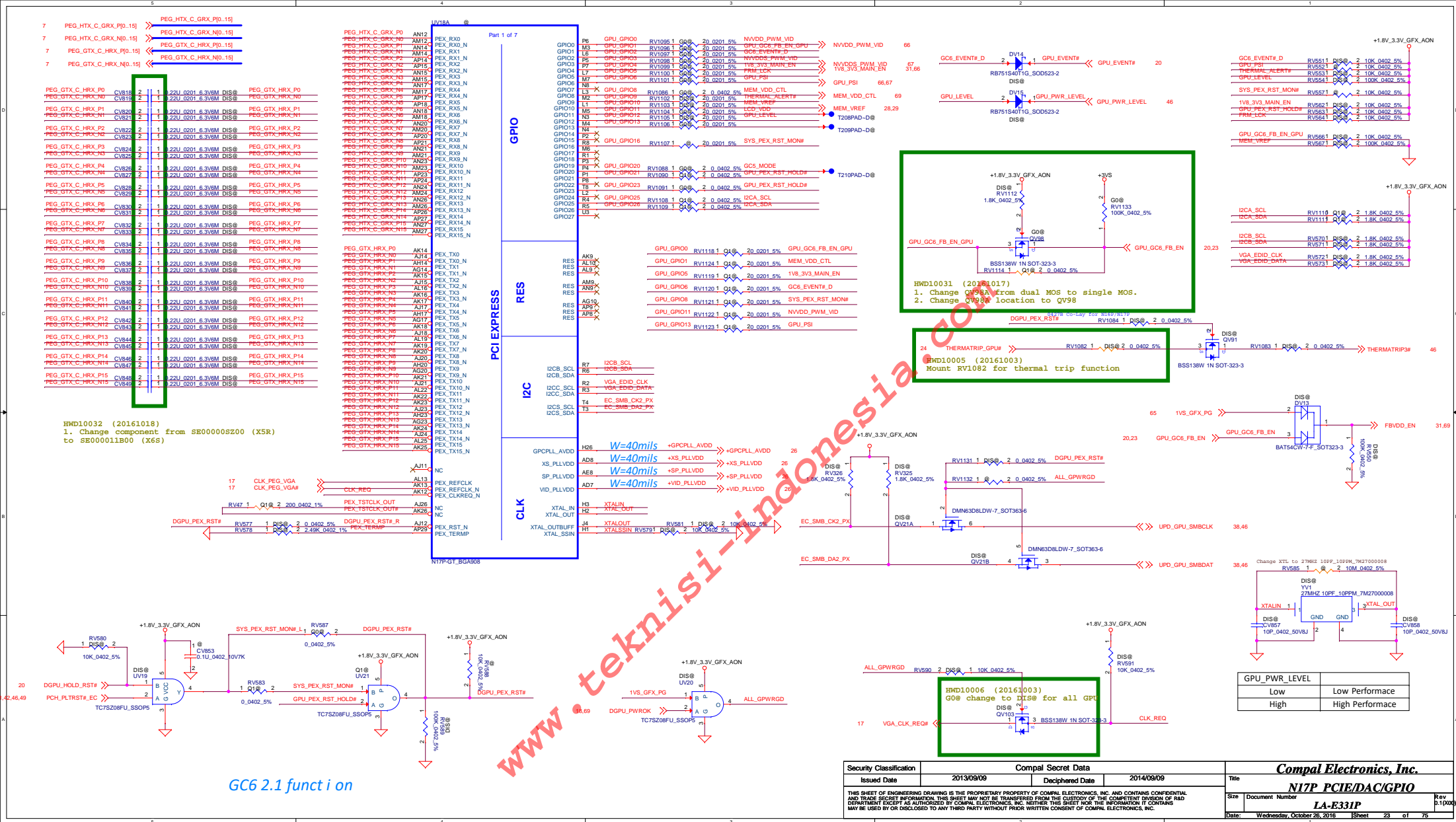


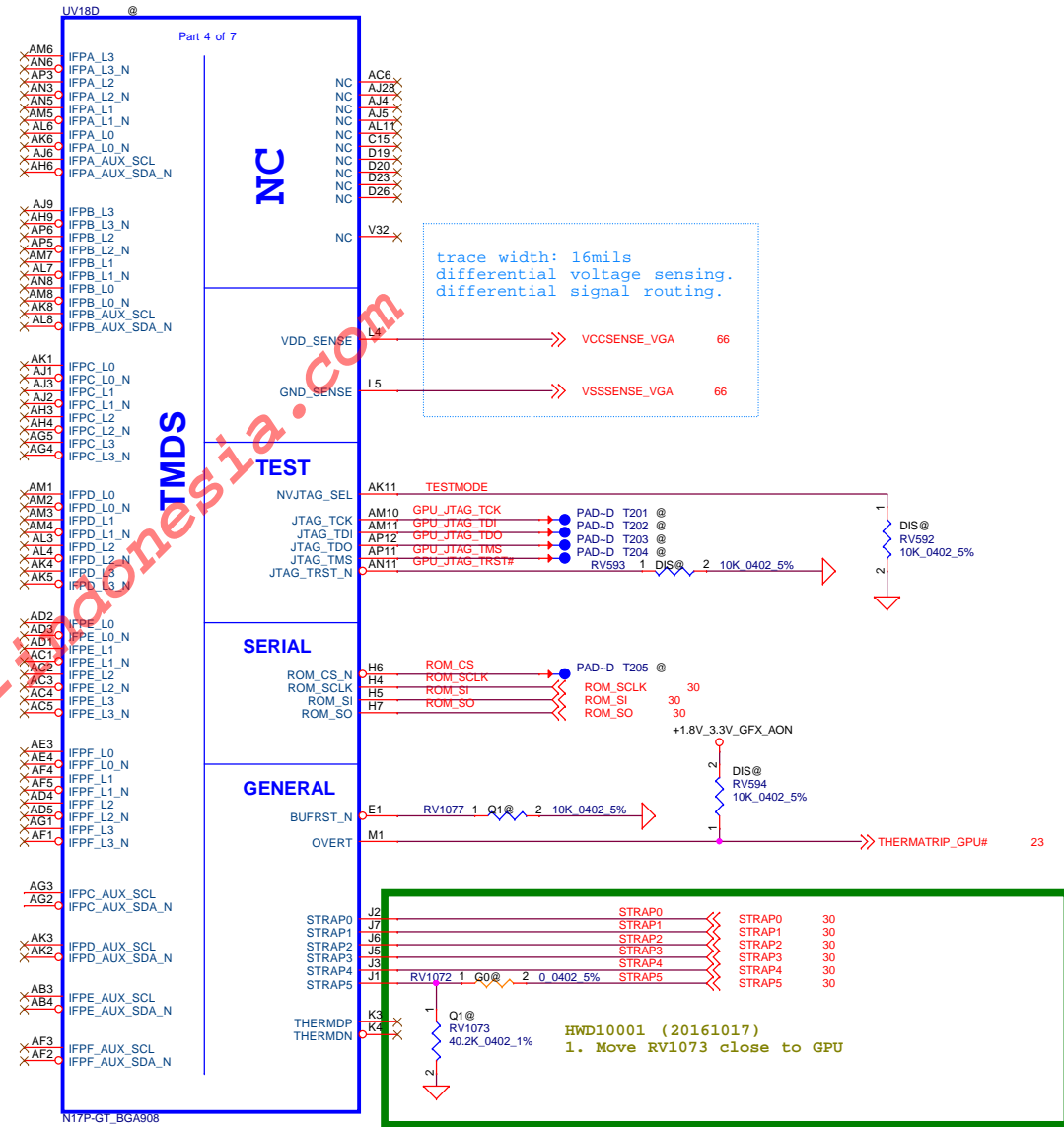




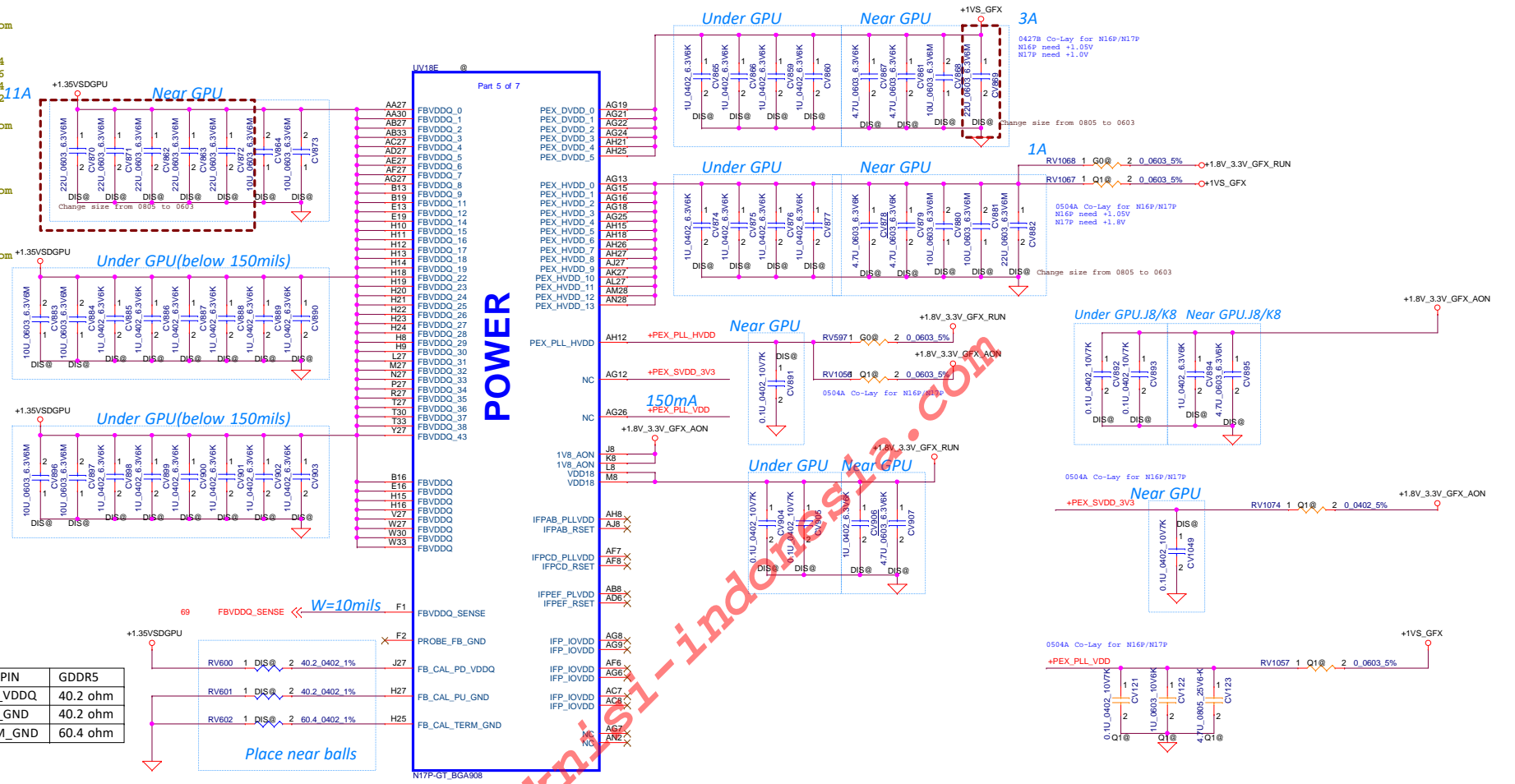
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				PCH (8/8) VSS			
				Size Document Number			Rev
				LA-E331P			0.1(00)
				Date: Wednesday, October 26, 2016			
				Sheet 22 of 75			

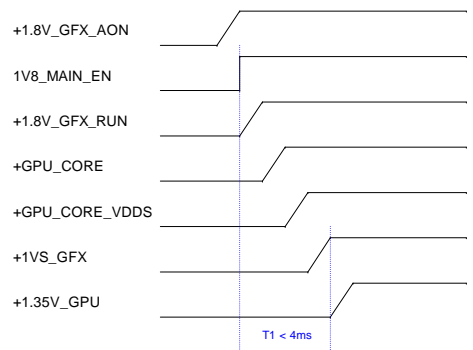




- HWD10032 (20161018)
1. Change below component from SE000000K80 (X5R) to E00001EP00 (X7R)
CV859, CV860, CV865, CV866, CV874
CV875, CV876, CV877, CV885, CV886
CV887, CV888, CV889, CV890, CV894,
CV898, CV899, CV900, CV901, CV902,
CV903
2. Change below component from SE000005T80 (X5R) to SE000010T00 (X6S)
CV864, CV873, CV880, CV881
CV883, CV884, CV896, CV897
3. Change below component from SE00000M000 (X5R) to SE00001CA00 (X6S)
CV863, CV869, CV870, CV872
CV882, CV924
4. Change below component from SE107475K80 (X5R) to SE00000G300 (X6S)
CV878, CV879, CV895

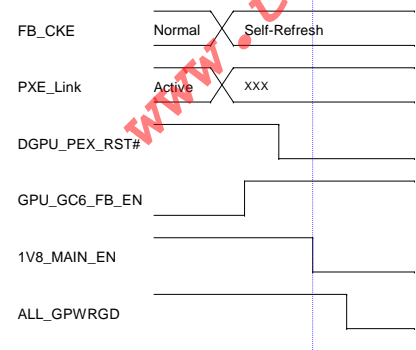


GPU Power Up Sequence



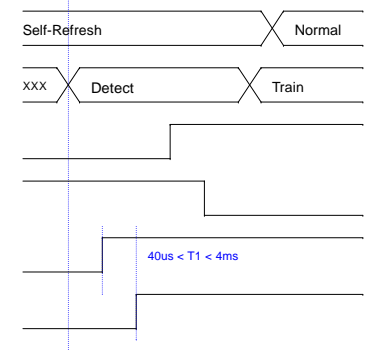
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

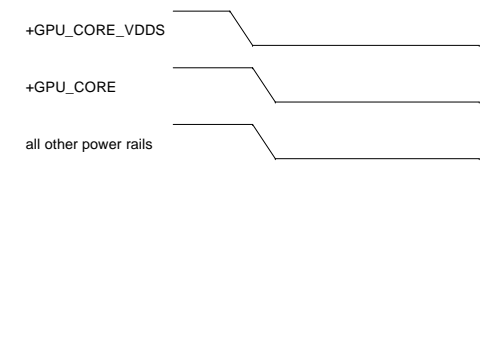


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



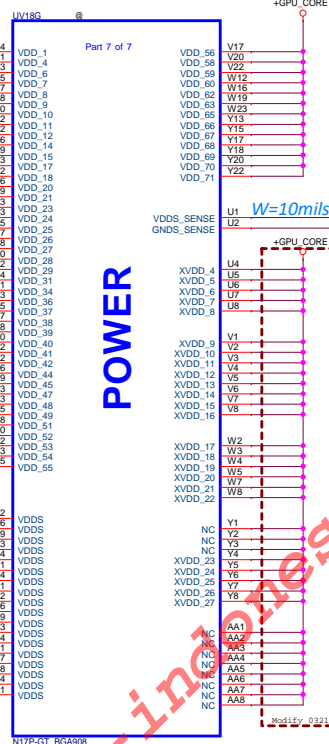
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2014/09/09	Title	N17P Power
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				LA-E331P	
				Rev	0.1000
				Date	Wednesday, October 26, 2016
				Sheet	25 of 75



0504A Co-Lay for N16P/N17P

47A +GPU_CORE

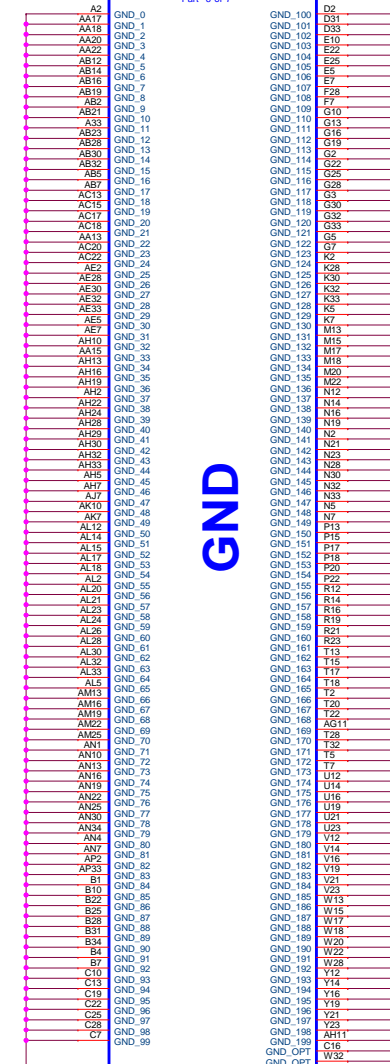
19A +GPU_CORE_VDD5



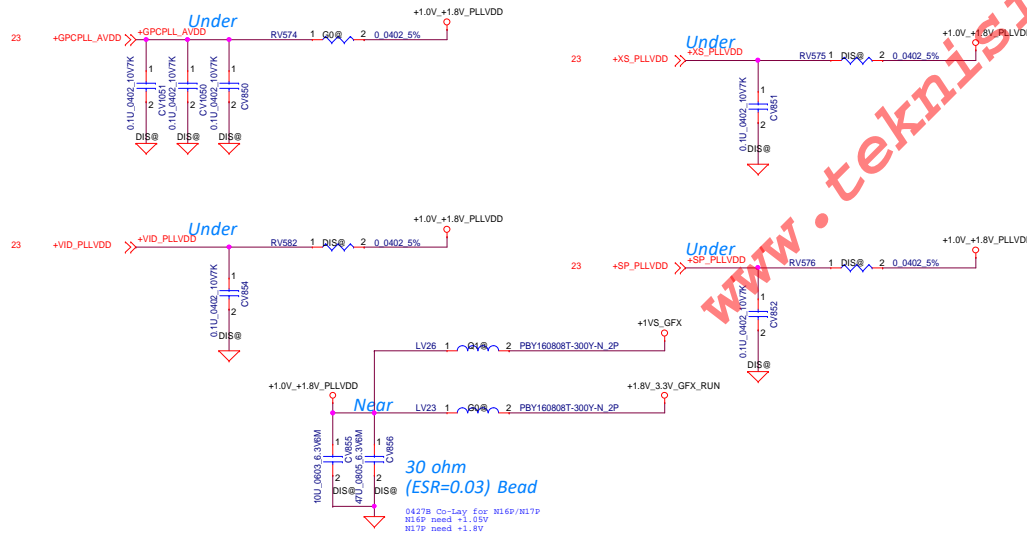
N17P-G1_BGA908

UV18F @

Part 6 of 7

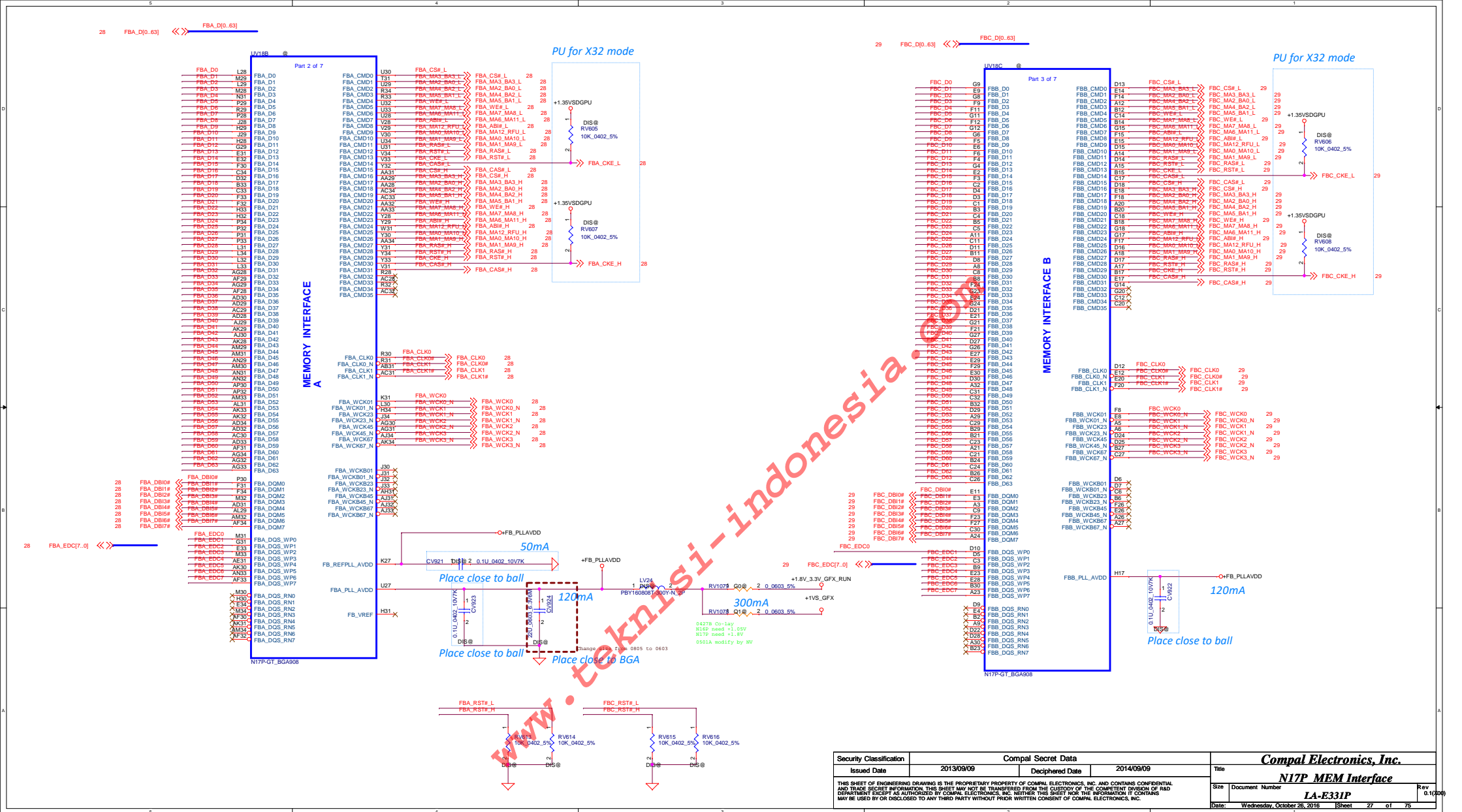


N17P-G1_BGA908



0427B Co-Lay for N16P/N17P
N16P need +1.05V
N17P need +1.8V

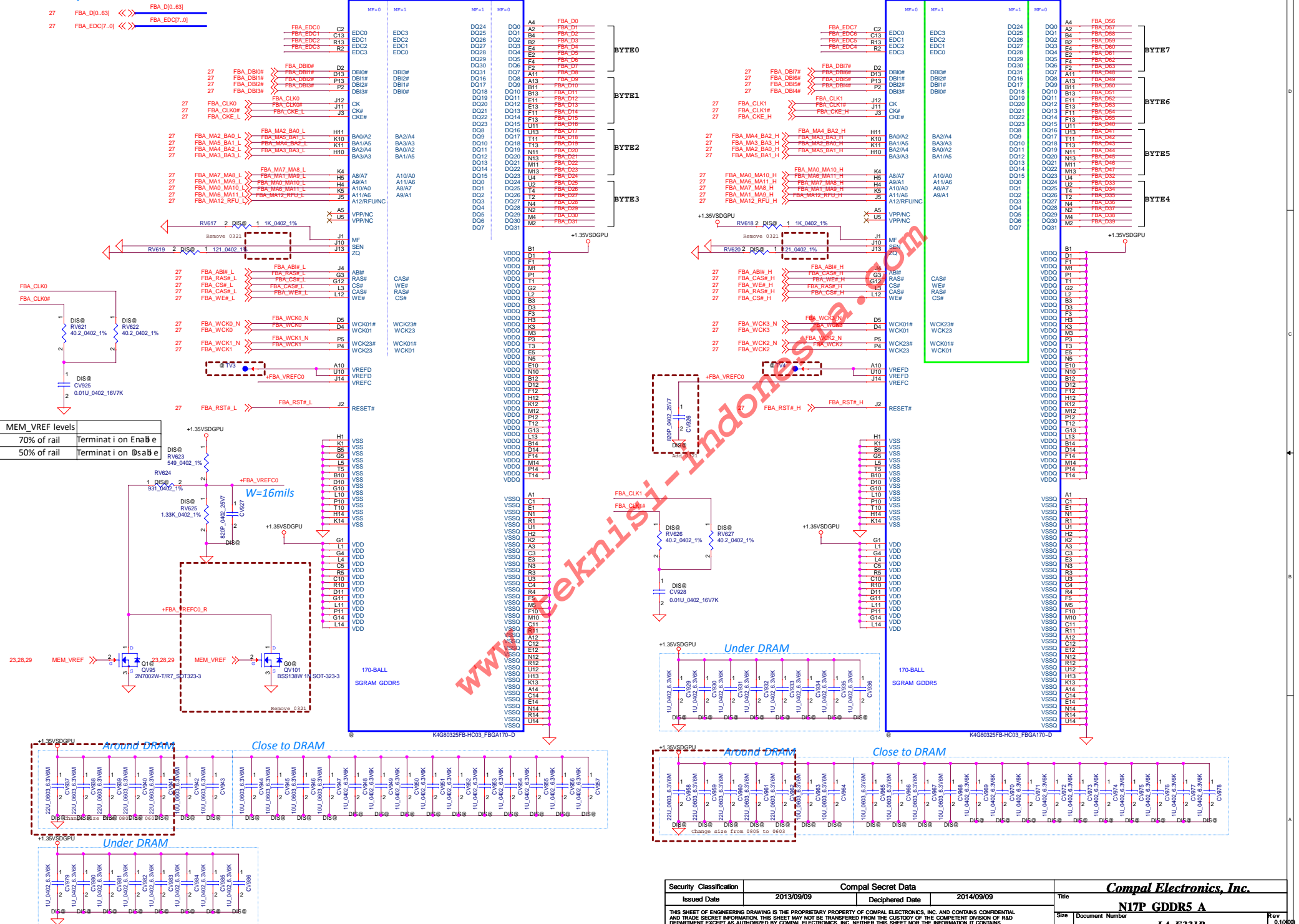
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Size	Document Number	LA-E331P	Rev	0.1000
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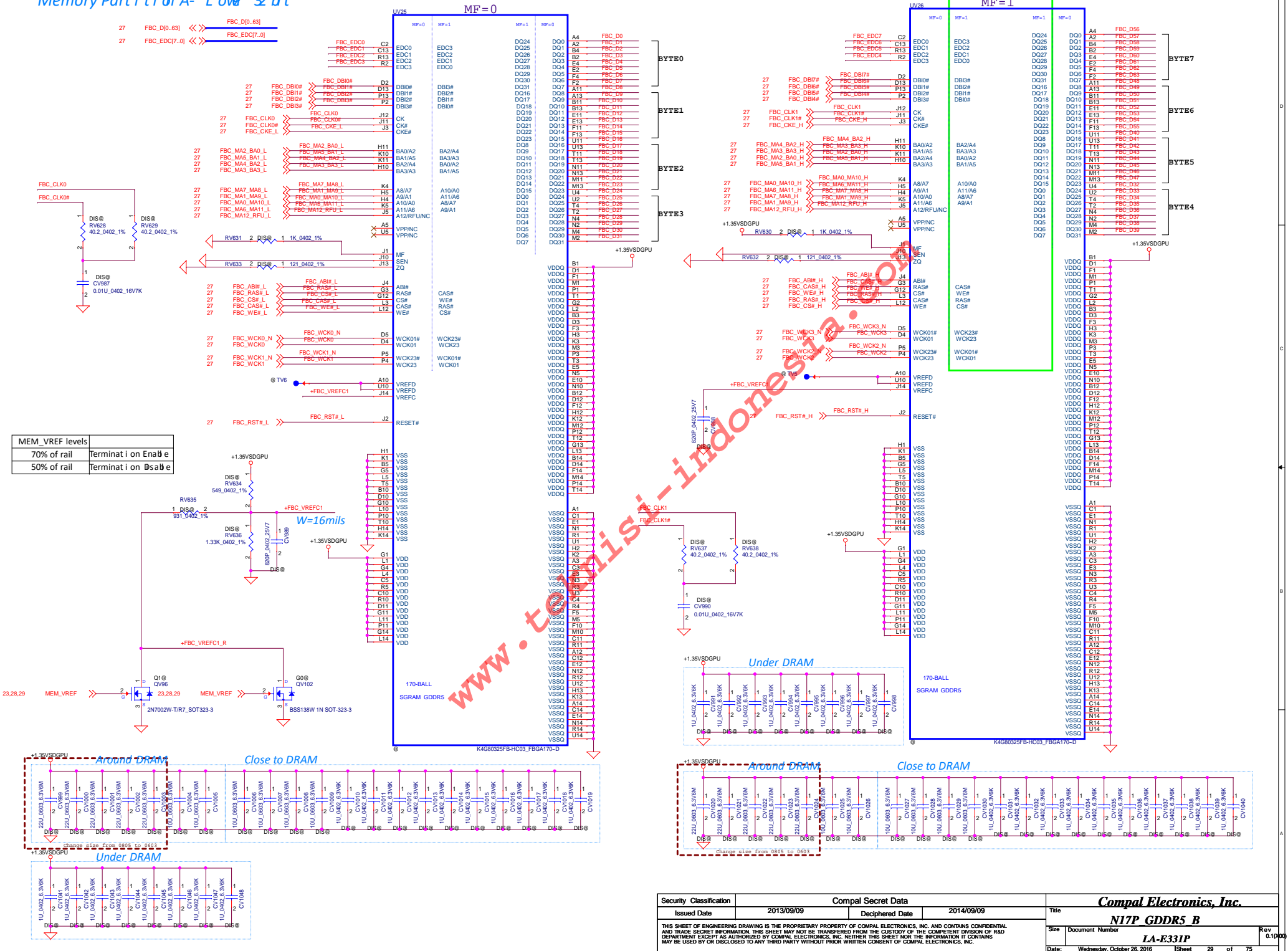
Memory Partition A- Low 32b

MF=0

MF=1



Memory Partition A- Low 32 bit



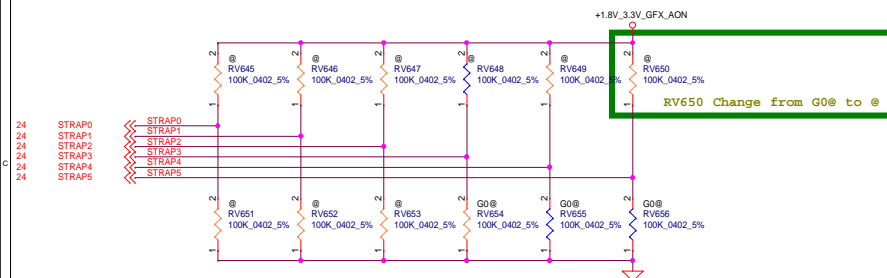
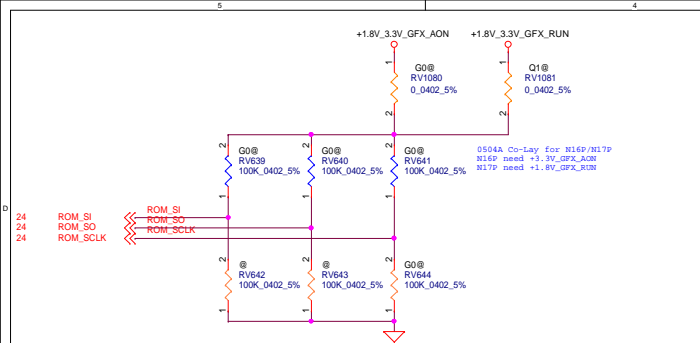


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000 SAMSUNG	0000
10.0 kΩ	1001 MICRON	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 4. N17P-Q1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	6 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x9	6 Gbps	N/A	Full	Production candidate

Notes:

- For N17P-Q1, the maximum allowable memory case temperature is 85 °C.

Table 1. N16P-Q3 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (Gbps)	Qual Freq (MHz)	Date Code Alert	Qual Plan	ETA
8 Gb	256Mx32 ²	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	5 Gbps	2500	N/A	Full	Done
			Micron	MT51J256M32HF-60:A	A-die	0x9	5 Gbps	2500	N/A	Full	Done

Notes:

- For N16P-Q3, the maximum allowable memory case temperature is 85 °C.
- 8 Gb is supported in x32 configuration only (no x16 support planned).

SMB_ALT_ADDR	State	DEVID_SEL	State	PCIE_CFG	State	VGA_DEVICE	State
Low	Single GPU	Low	Original Device ID	Low	Normal signal swing	Low	3D Device
High	Dual GPU	High	Re-brand Device ID	High	Reduce the signal amplitude	High	VGA Device

Table 5.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	HYNIX

N17P-G0/-G1 GDDR5 MEMORY RVL

NVIDIA recommends the following GDDR5 memories for use in conjunction with notebook designs using N17P-G0/-G1 GPUs.

Table 1. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Type	FBVDD/FBVDDQ	Memory Density	Allowed Memory Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V and 1.5V/ 1.5V See Note 2	8 Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	0x0	3500	N/A	Production candidate
				Micron	MT51J256M32HF-70:A	A-die	0x1	3500	N/A	Production candidate
				Hynix	H5GQ8H24MR-R0C	M-die	0x2	3500	N/A	Post-production candidate

Note:

- For N17P-Gx, the maximum allowable memory case temperature is 85 °C.
- N17P-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DV5 is required to run WCLK > 3000 MHz.

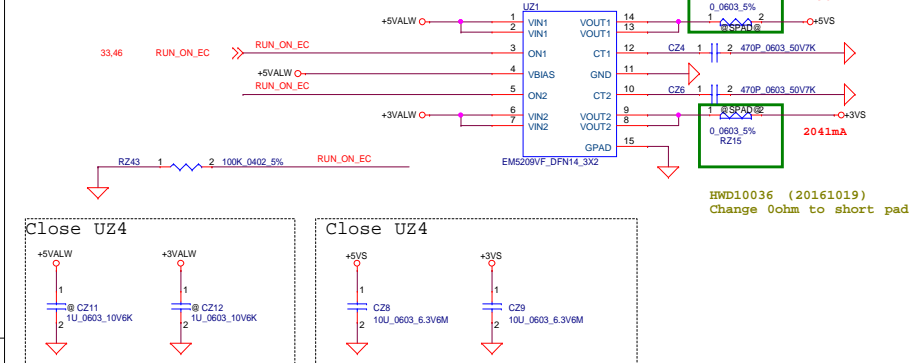
Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND.			
STRAP2	Do not stuff.			
STRAP3				
STRAP4				

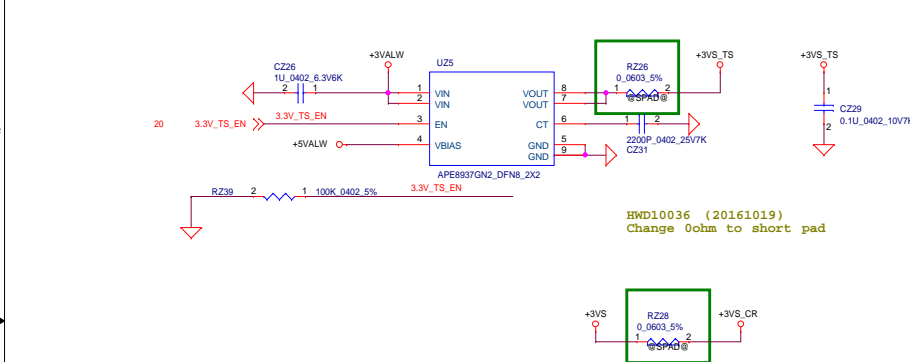
Berlinetta MLK			
Straps	(N17P-Q1)	(N17P-G0)	
Net NAME	state	State	defind
ROM_SCLK	PD 5K	"M"	SOR_EXPOSED(LSB)
ROM_SI	Base on memory RVL.	"H"	SOR_EXPOSED
ROM_SO	PD 5K	"H"	SOR_EXPOSED(MSB)
STRAP0	PU 49.9K		RAMCFG(LSB)
STRAP1	Do not stuff		RAMCFG
STRAP2	Do not stuff		RAMCFG(MSB)
STRAP3	Do not stuff	"L"	SMB_ALT_ADDR(0), DEVIE_SEL(0)
STRAP4	Do not stuff	"L"	PCIE_CFG(0), VGA_DEVICE(0)
STRAP5	Unused	"L"	

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Size C	Document Number	LA-E331P		Rev	0.1(000)
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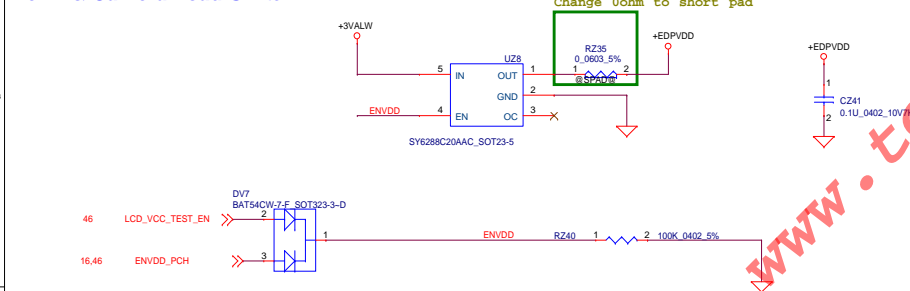
+5VALW to +5VS
+3VALW to +3VS



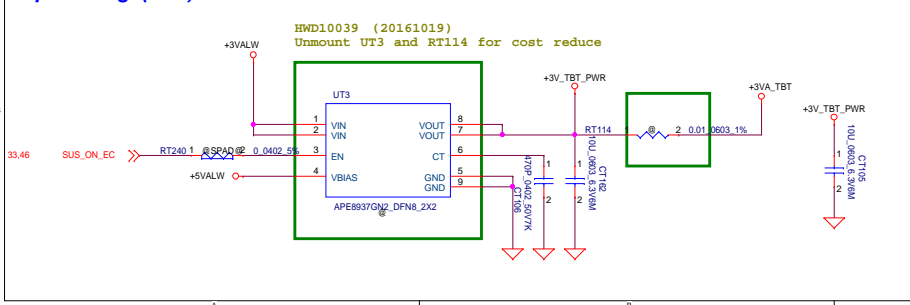
Touch Screen Load Switch & Card Reader



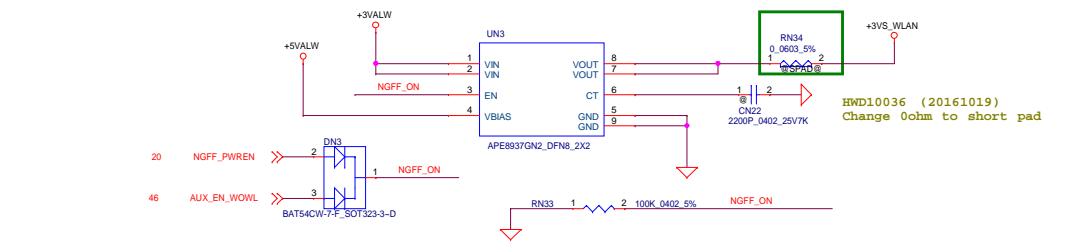
eDP & Camera Load Switch



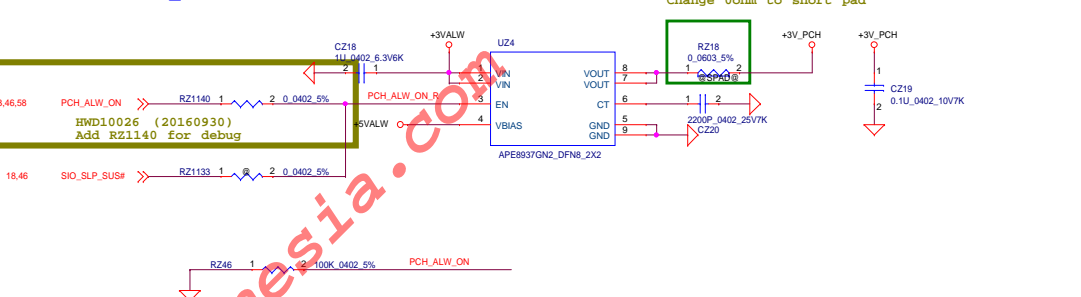
Alpine Ridge(TBT) Load Switch



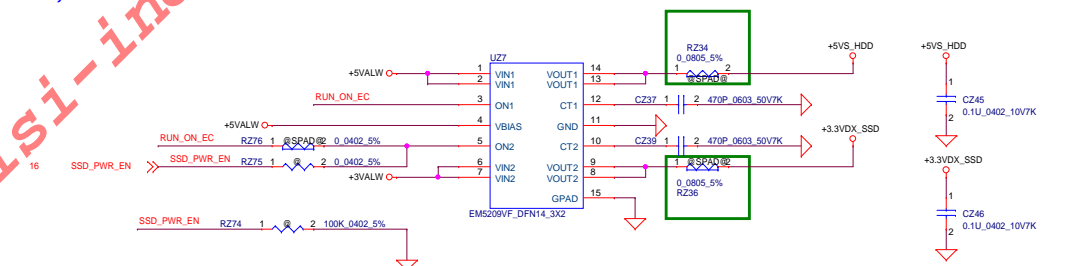
WLAN Load Switch



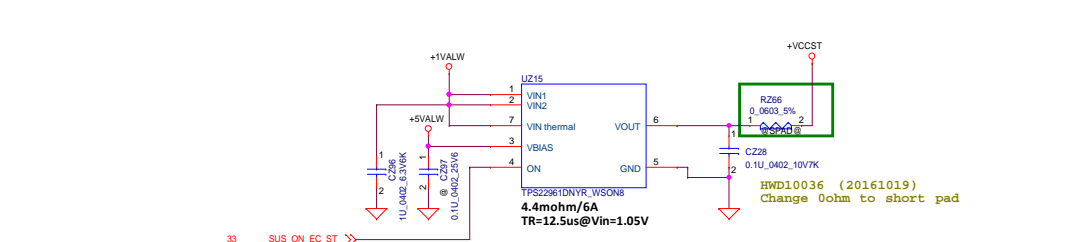
+3VALW to +3V_PCH



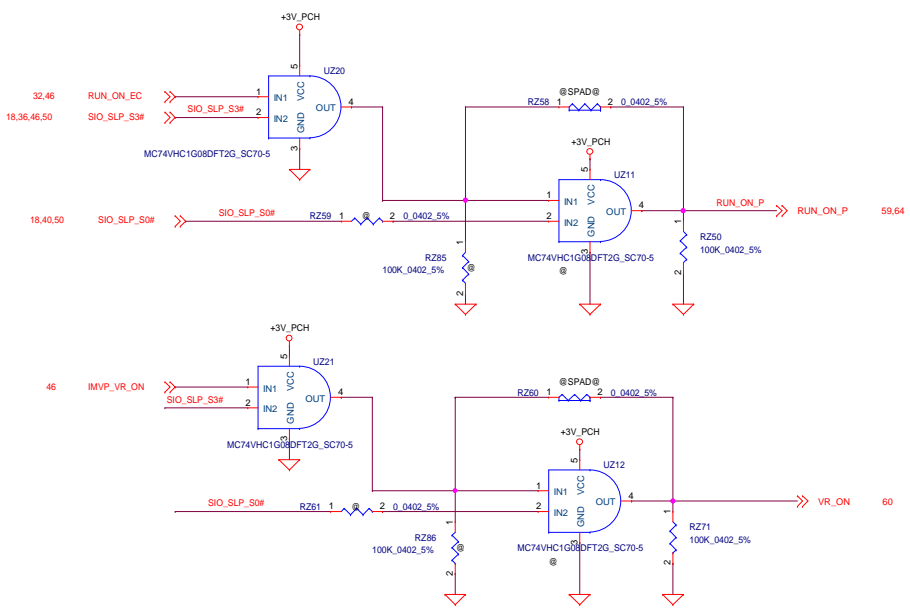
HDD, SSD Load Switch



+VCCST Load Switch

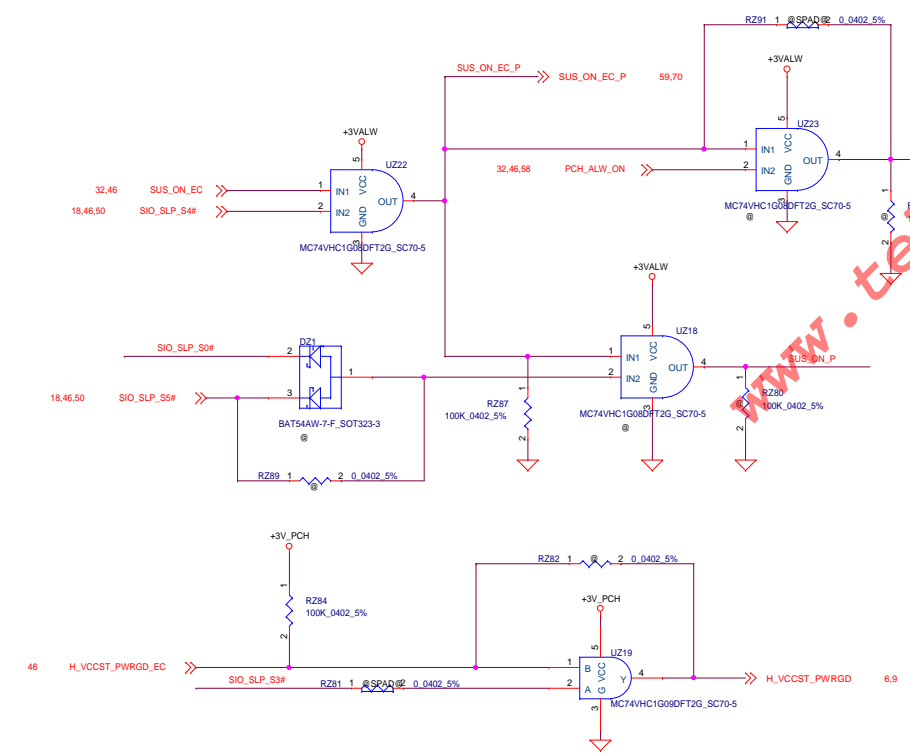


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						Size	Document Number		Rev
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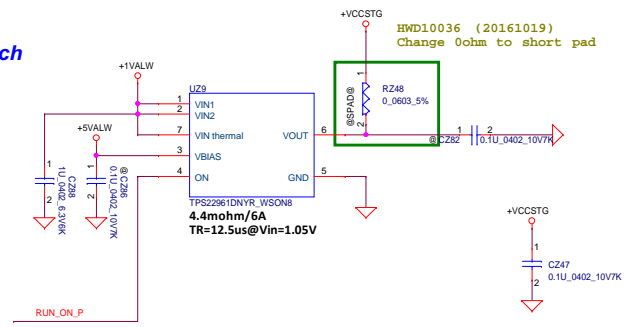


DDR4 VPP Load Switch

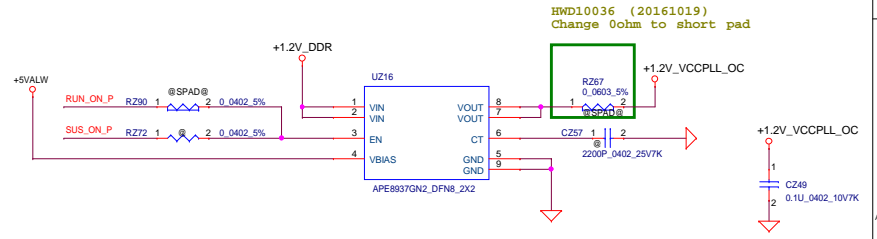
20160623 delete DDR4 VPP load switch change to PW p70



+VCCSTG Load Switch

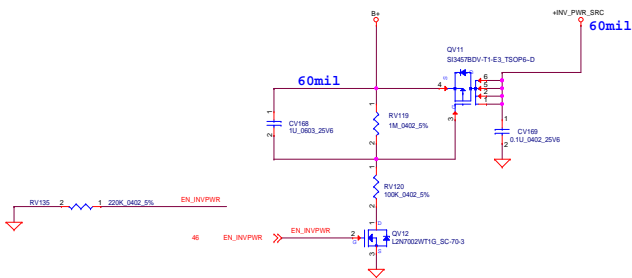


+VCCPLL_OC Load Switch

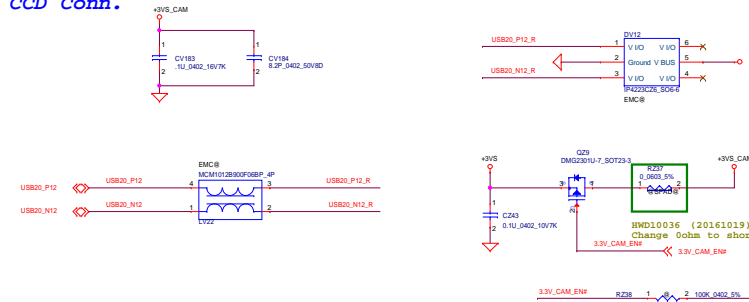


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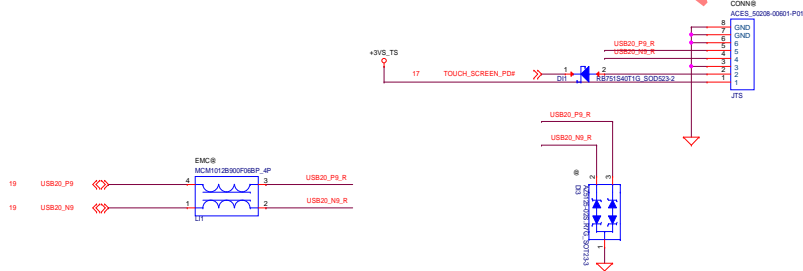
LCD backlight PWR CTRL



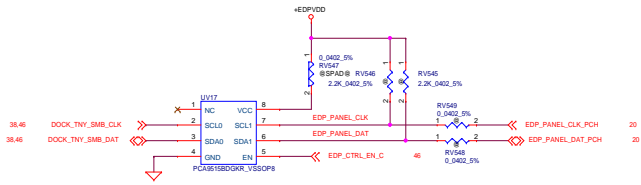
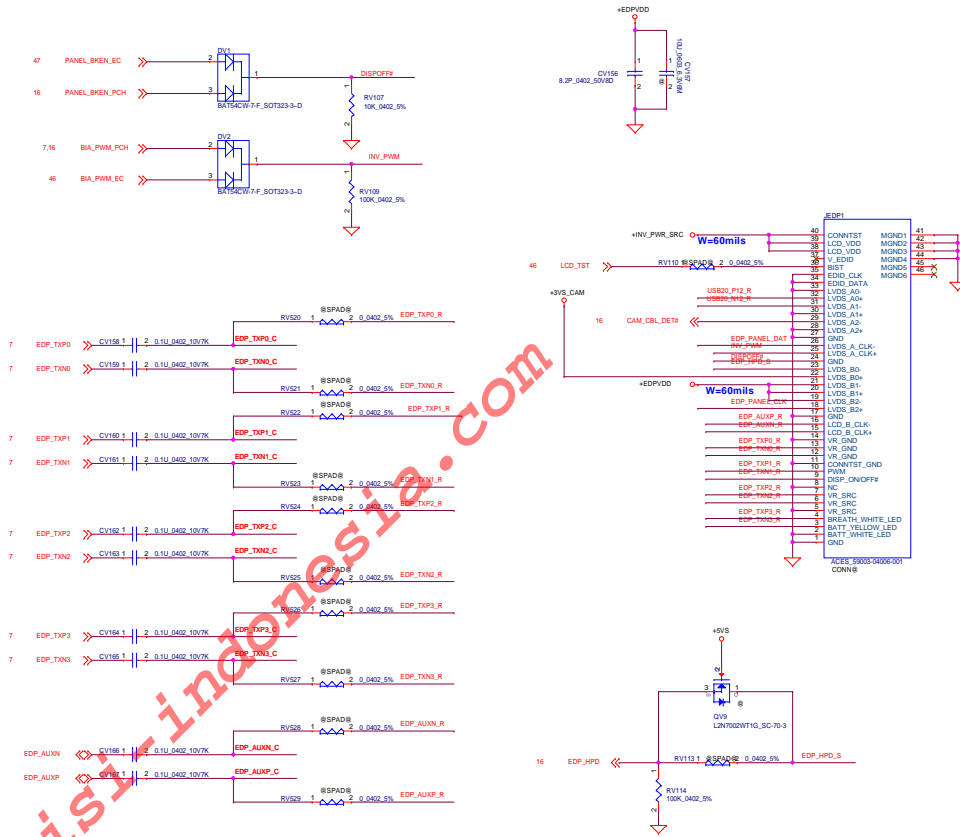
CCD Conn.



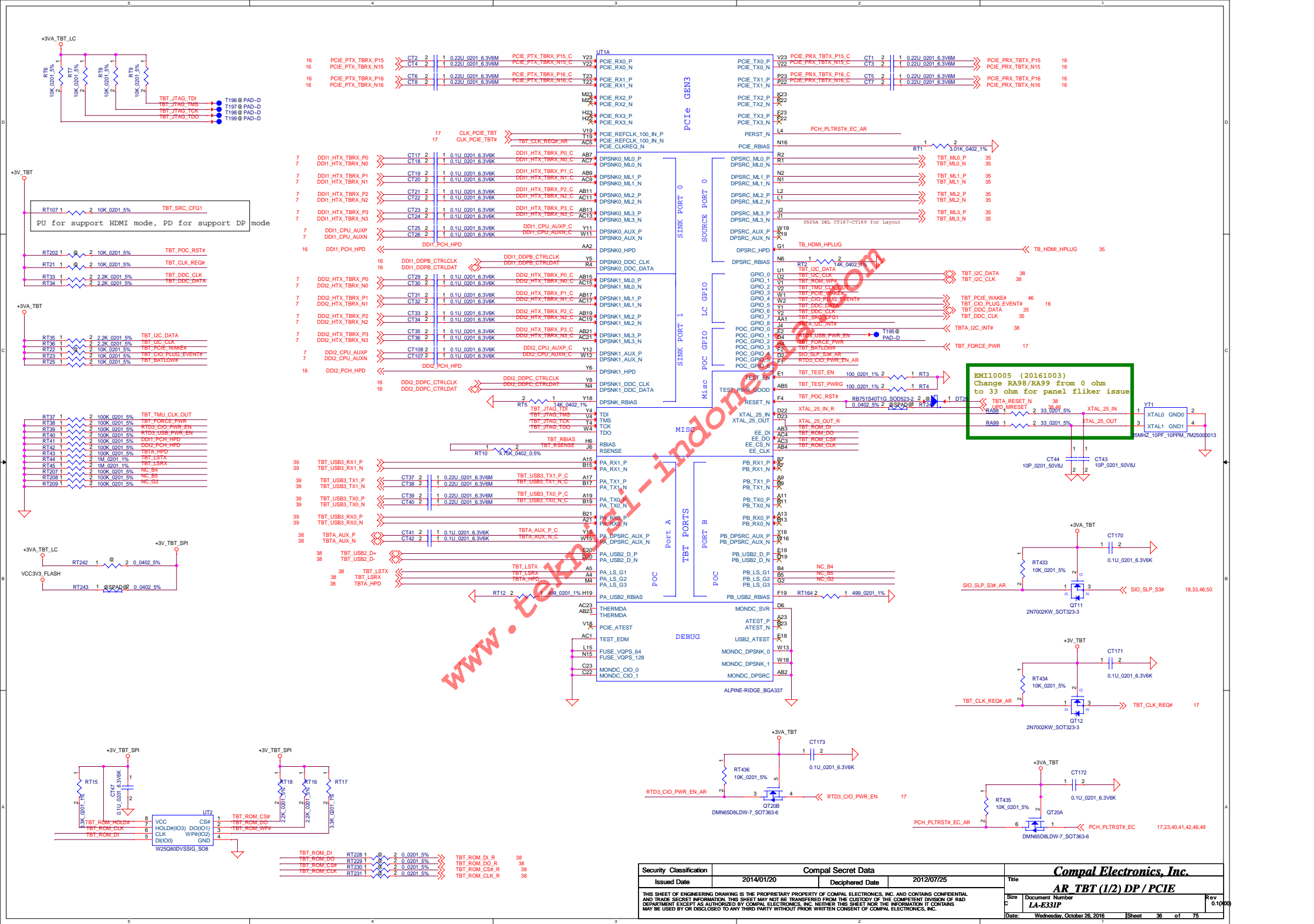
Touch Screen Conn.

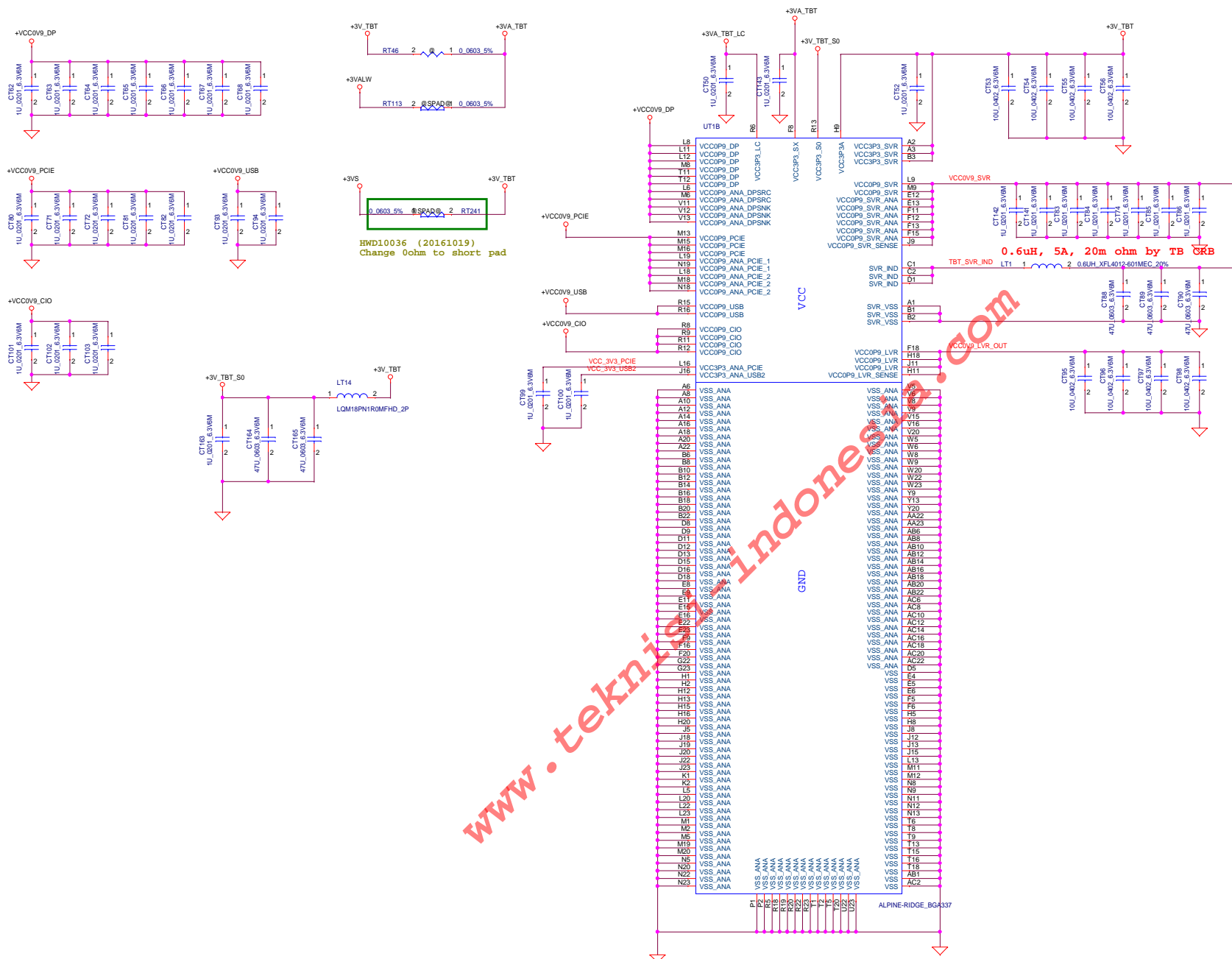


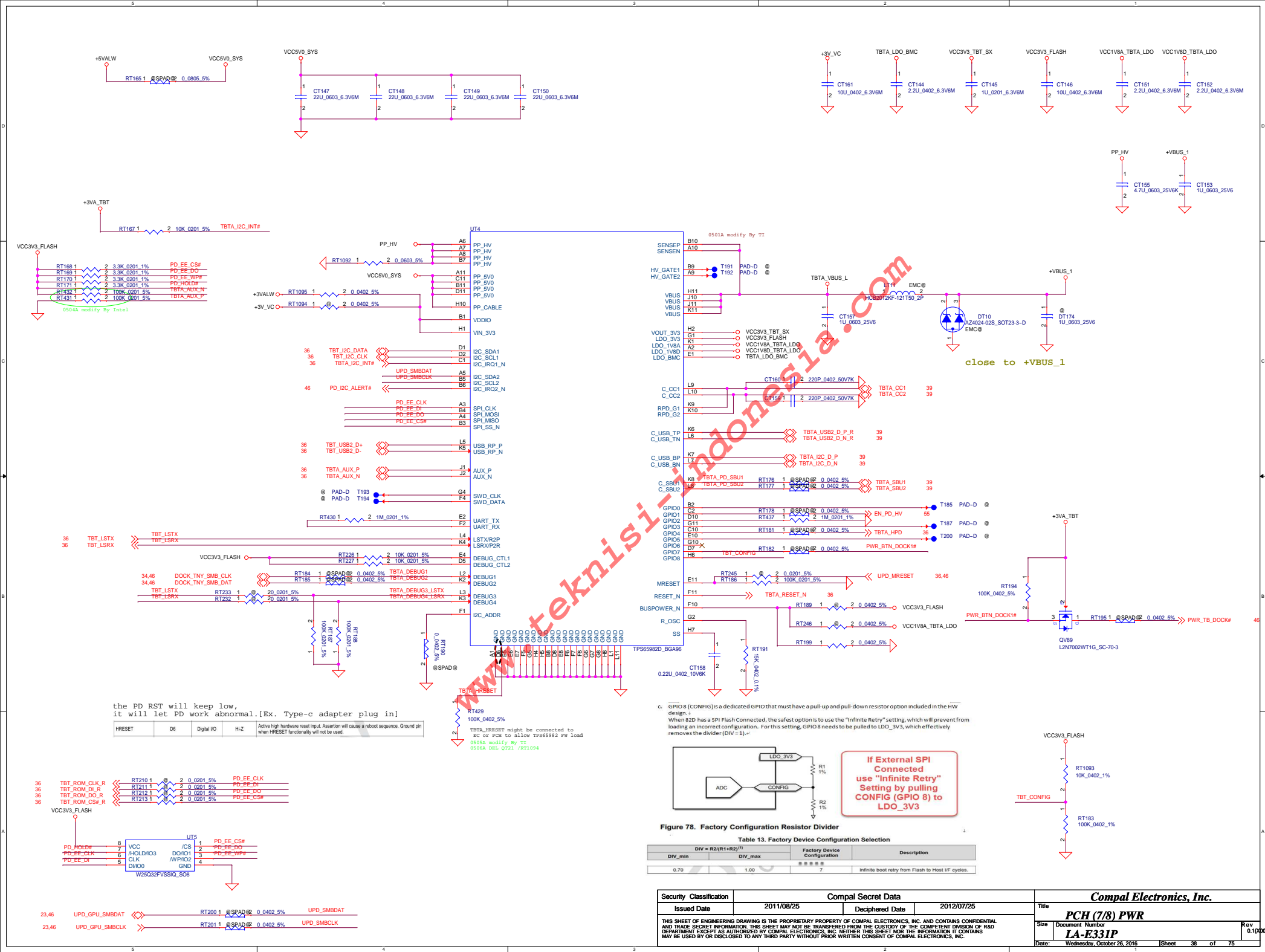
eDP & TS Conn.

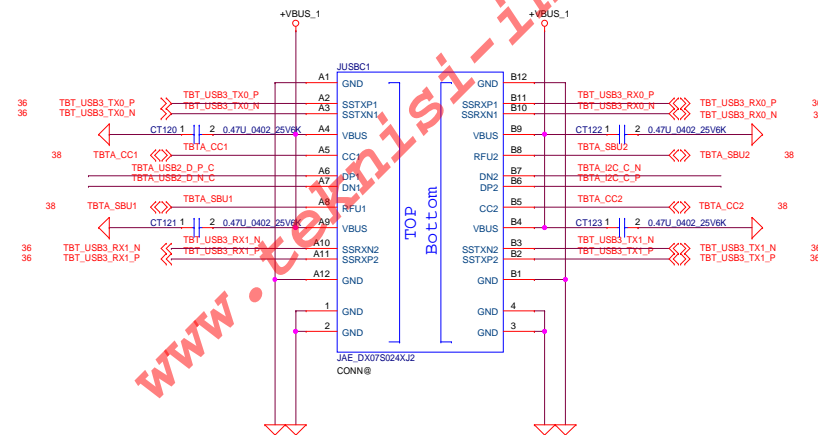
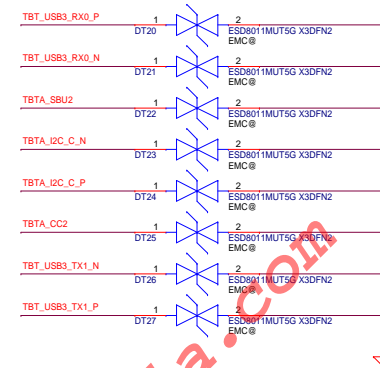


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				Size	Document Number	Rev
					LA-E33IP	0.1000
Date:				Wednesday, October 26, 2016	Sheet	39 of 75

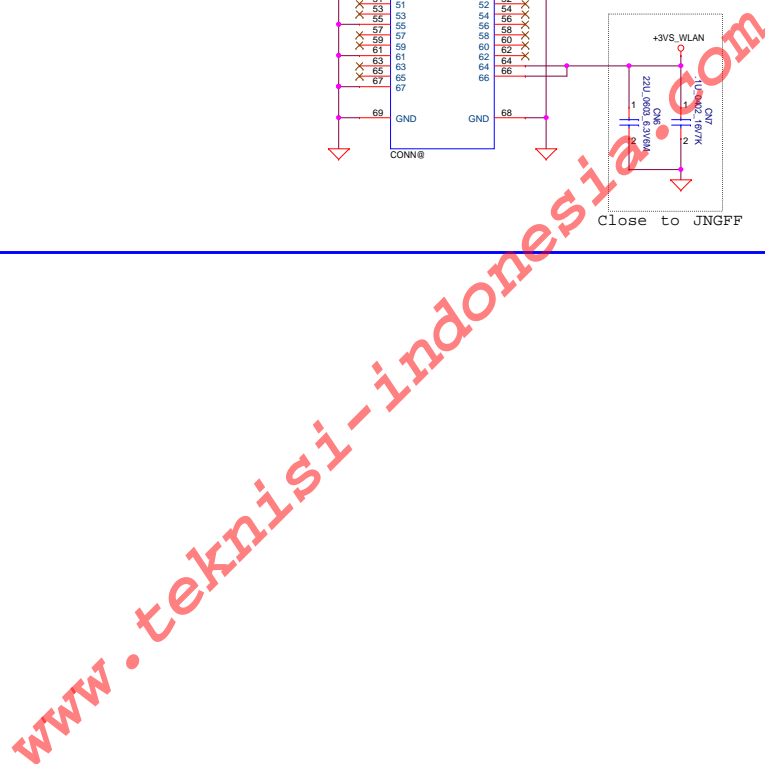
EMC@

MCM1012B900F06BP_4P

19 USB2.0_P4 4 3 USB2.0_P4_R

19 USB2.0_N4 1 2 USB2.0_N4_R

LN1

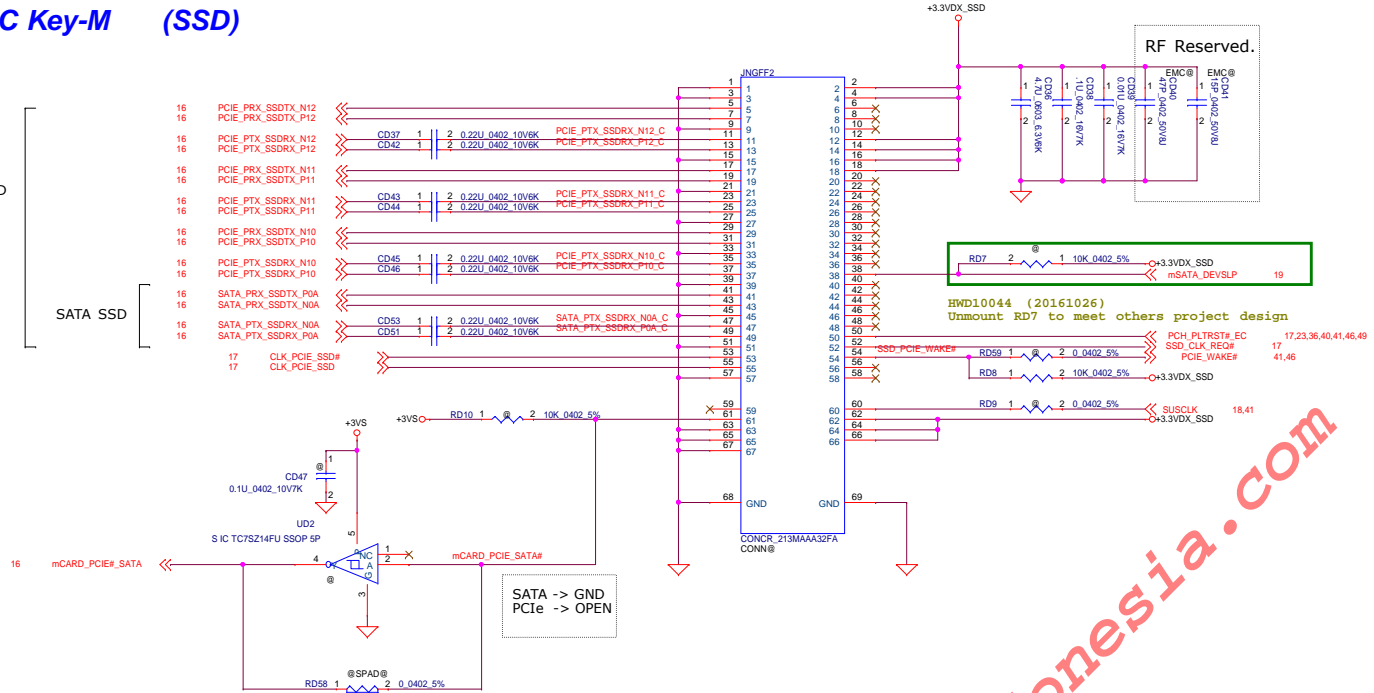


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				Date:	Wednesday, October 26, 2016
				Sheet	41 of 75

M.2 Slot-C Key-M (SSD)

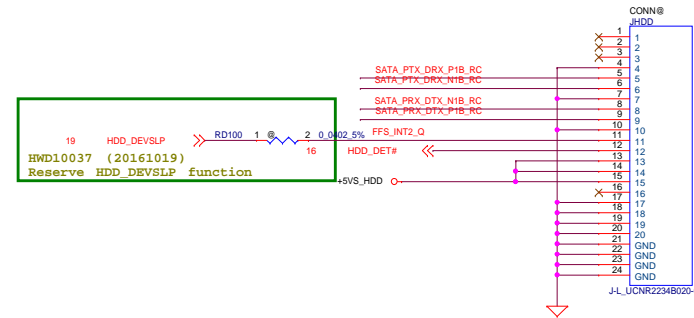


SATA SSD

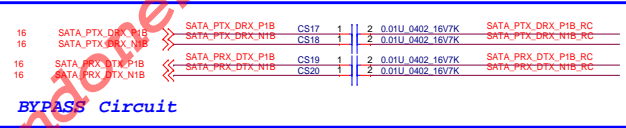
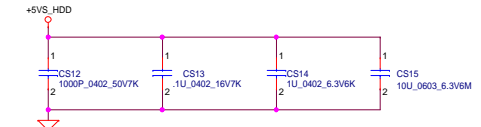


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					LA-E331P	0.1/000
				Date:	Wednesday, October 26, 2016	Sheet 42 of 75

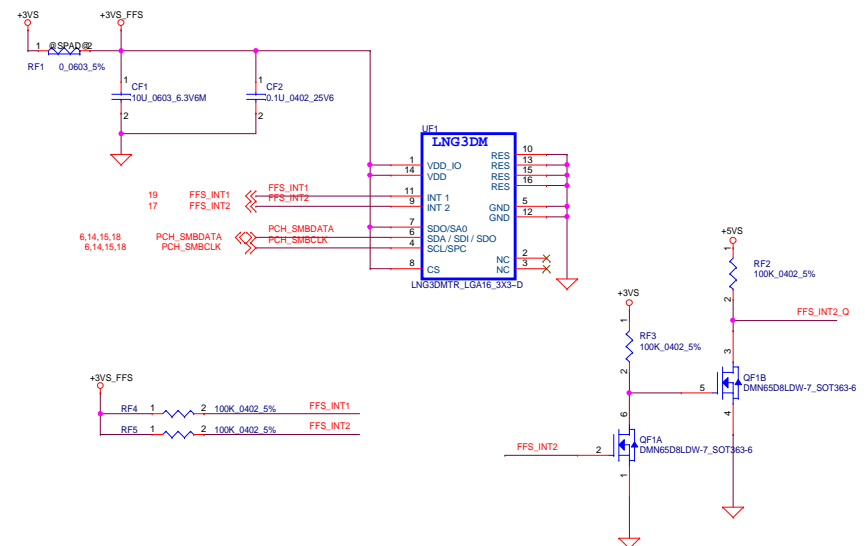
HDD CONN



Place near HDD CONN (JHDD1)



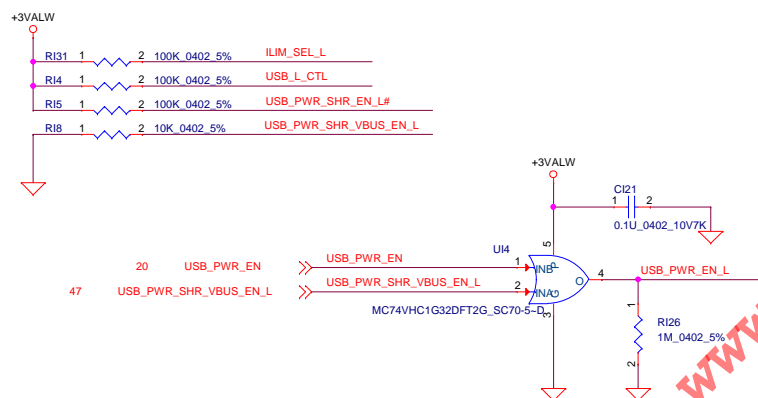
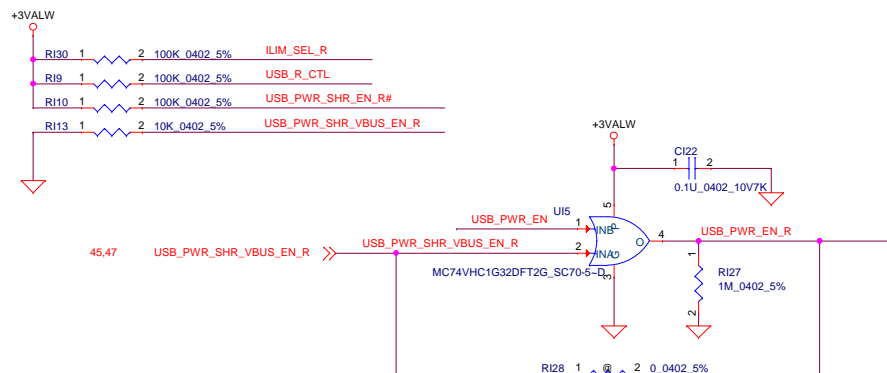
Free Fall Sensor



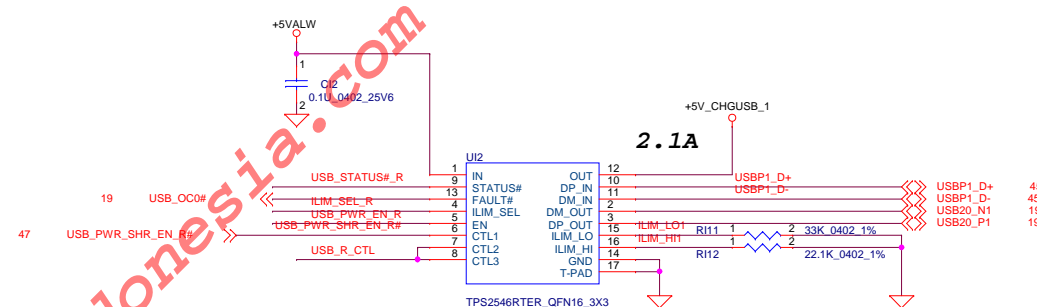
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

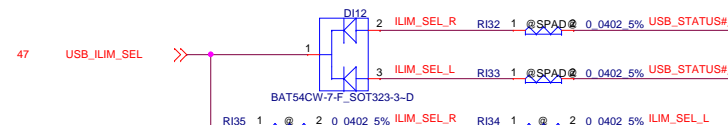
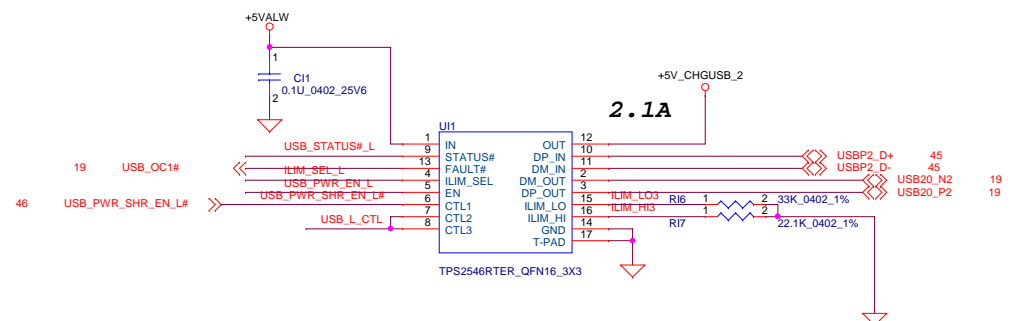
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)



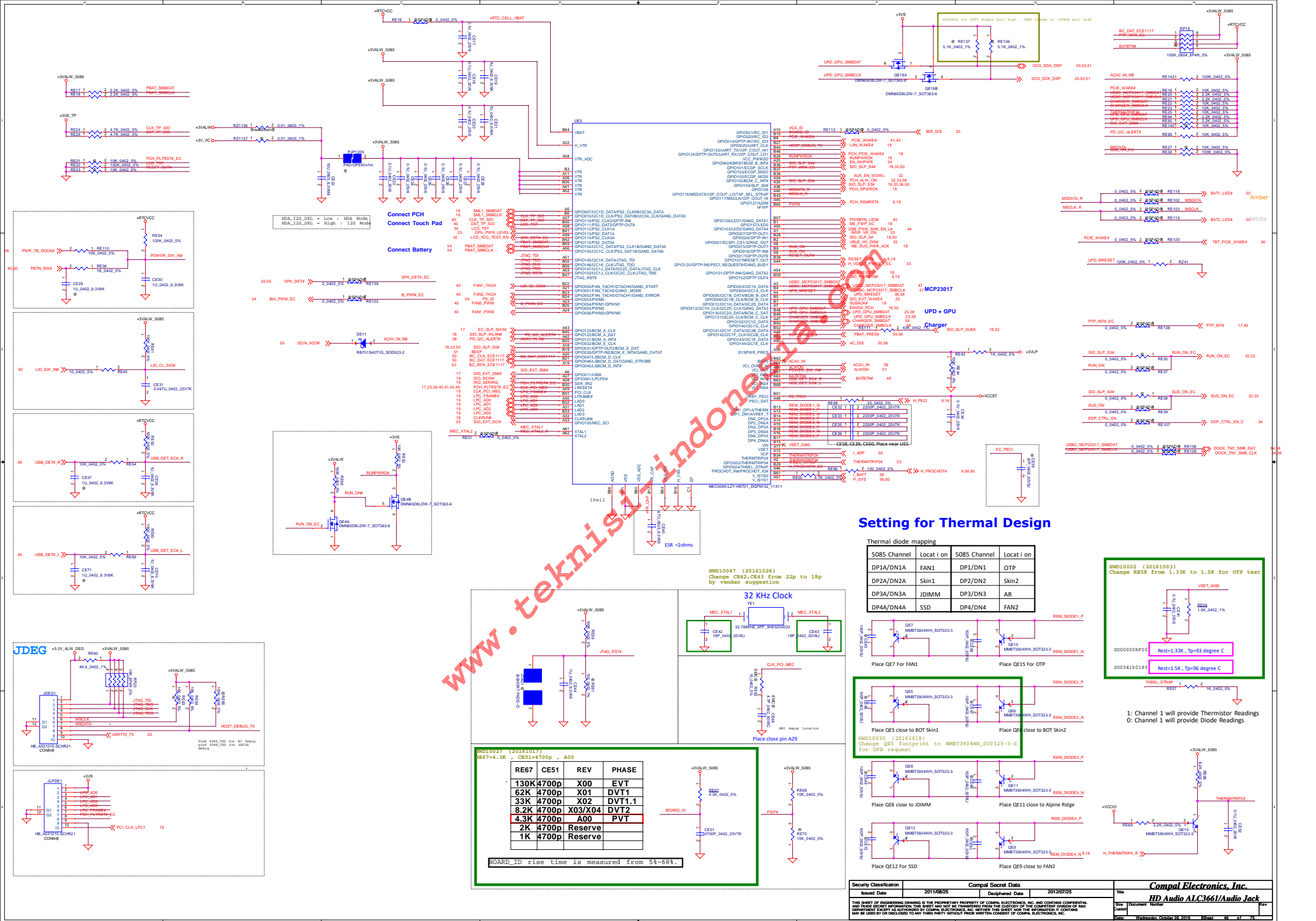
USB3.0 / USB2.0 Port1 (Right Side)

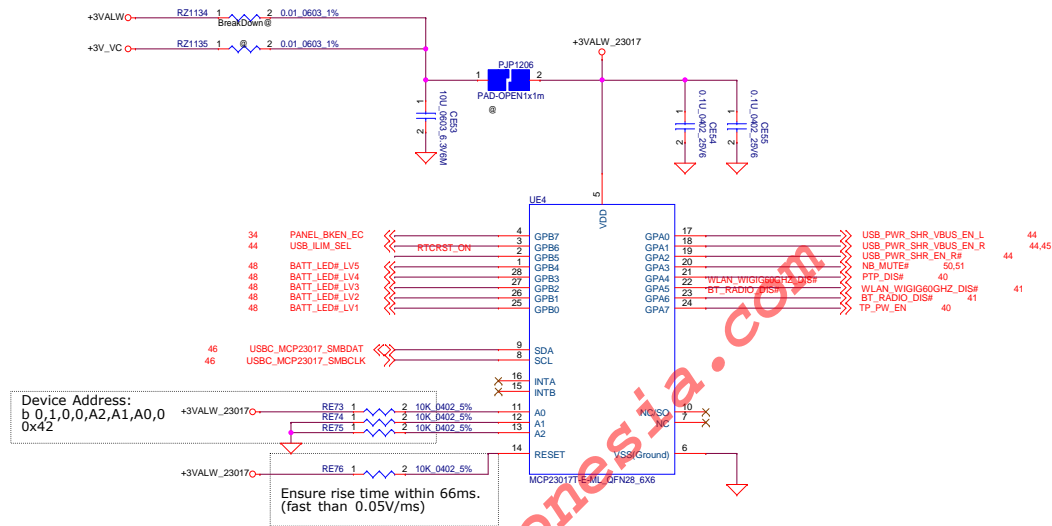
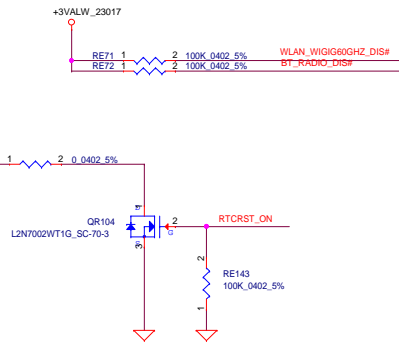


USB3.0 / USB2.0 Port2 (Left Side)



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				Size	Document Number
				LA-E331P	
				Date	Wednesday, October 26, 2016
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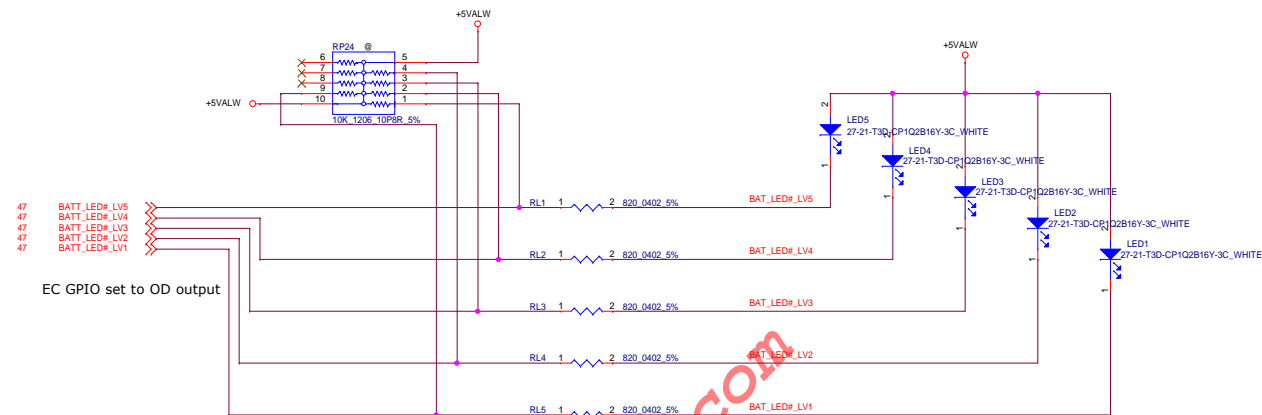
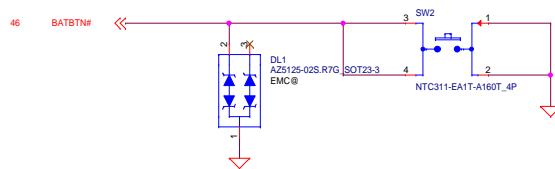




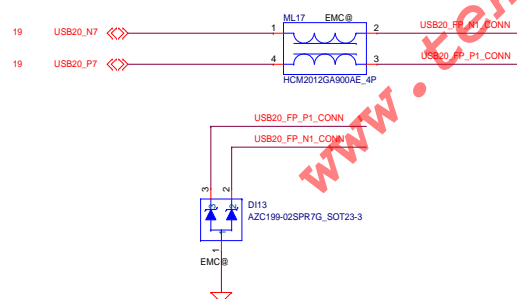
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/08/25		Title	
		Deciphered Date		2012/07/21	
				AMP TPA3113/SPK conn.	
				Size	
				Document Number	
				LA-E331P	
				Rev	
				0.1(200)	
				Date: Wednesday, October 26, 2016	
				Sheet 47 of 75	

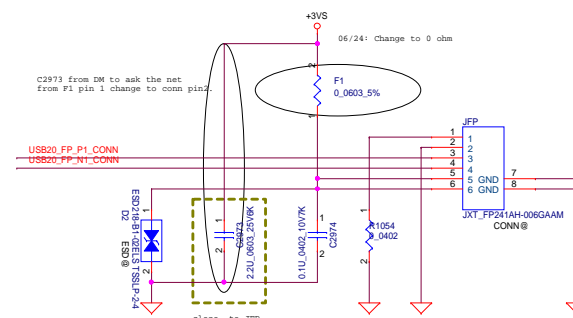
Bat t e r y G a u g e L E D



Fingerprint Reader CONN



```
( Fingerprint Reader )
Current capability: 3.3V 150mA
```



```

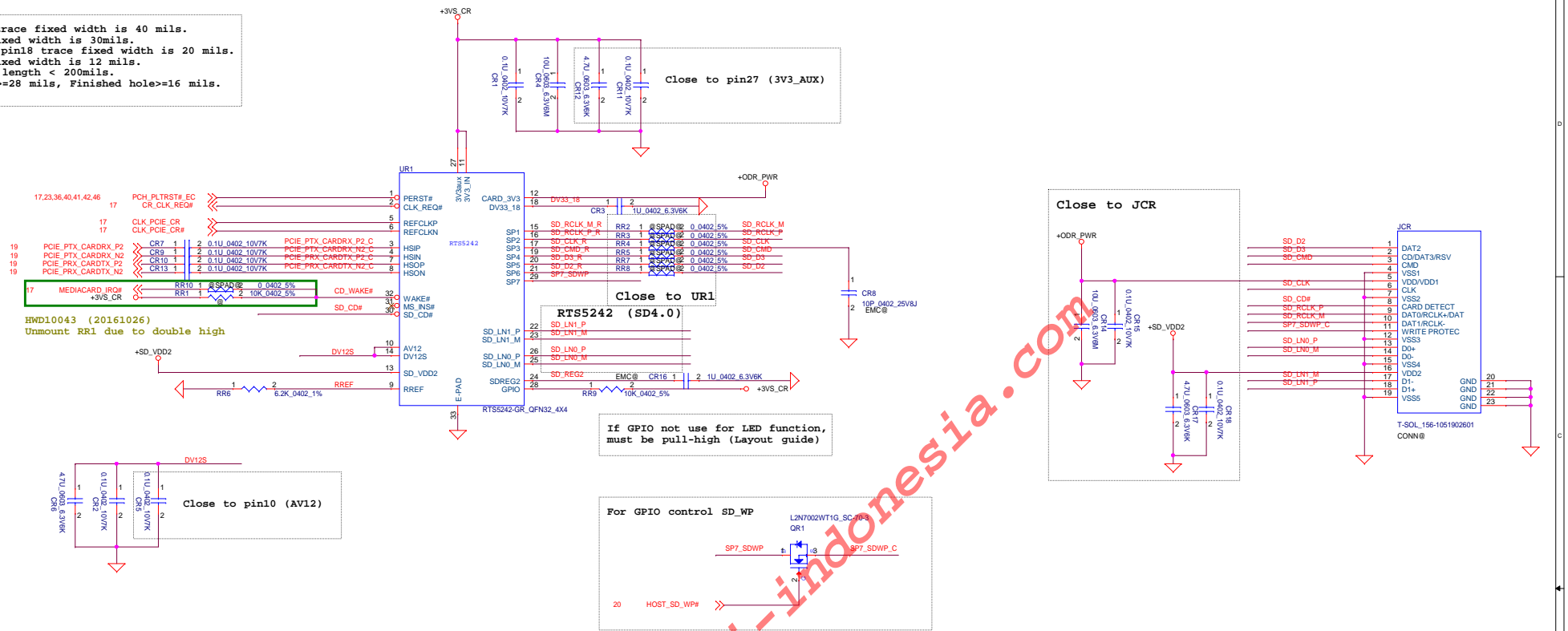
12/10 : JFPR1 Follow ME P/N and CIS SP01001Y900
12/28 : FPR connect pin define mirror vertically for BOT side

```

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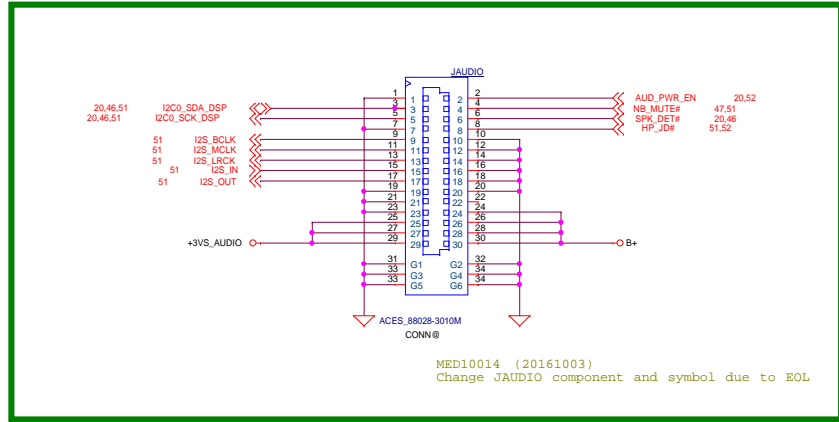
Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.

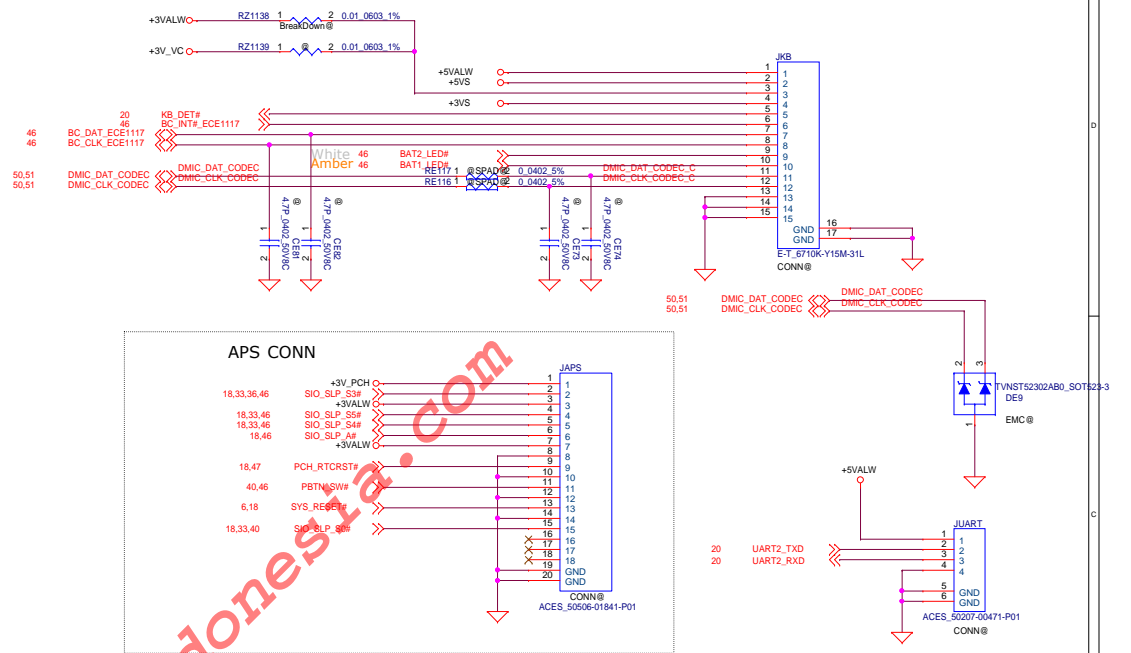


AUDIO Board Conn.

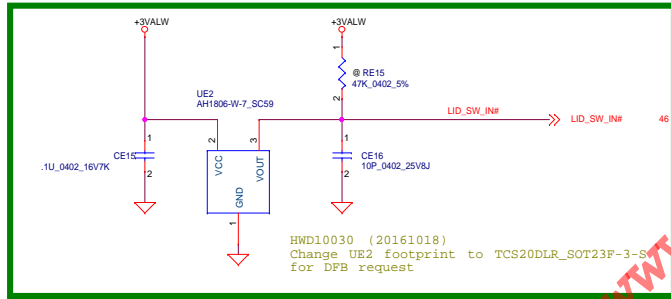
20160415 follow berlinetta broad to broad CONN



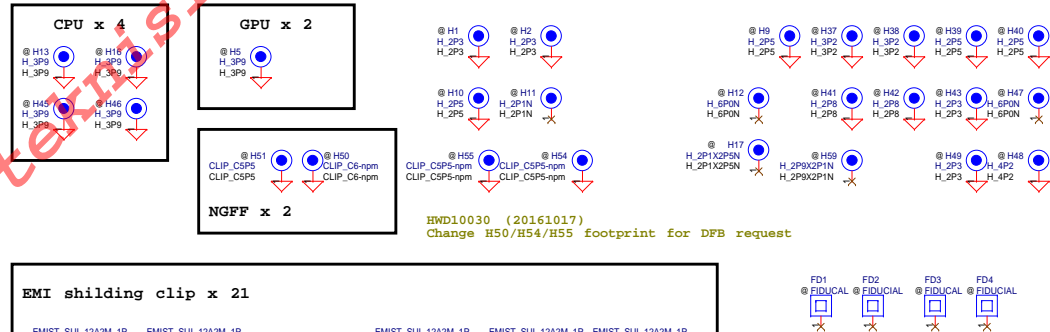
Keyboard Controller board + DMIC



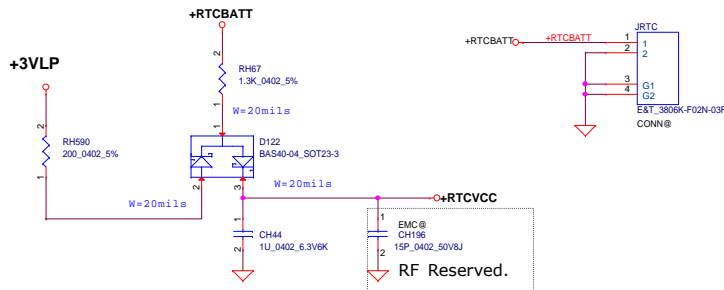
Lid Switch



Screw Hole

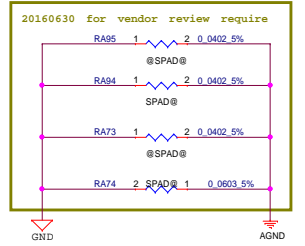
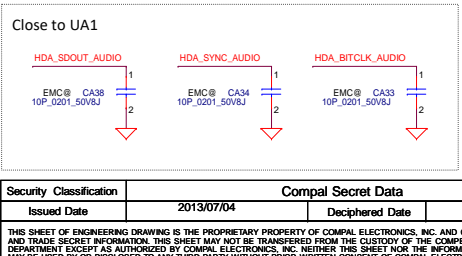
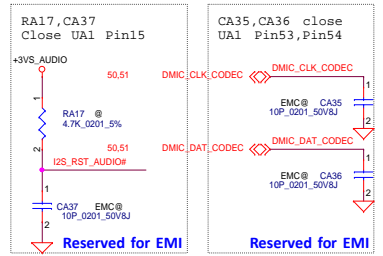
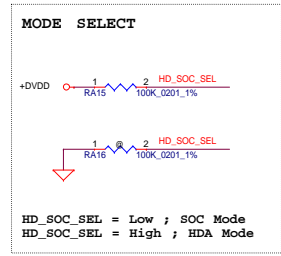
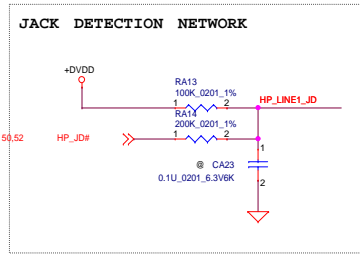
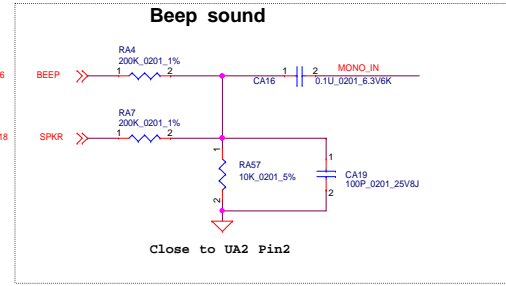
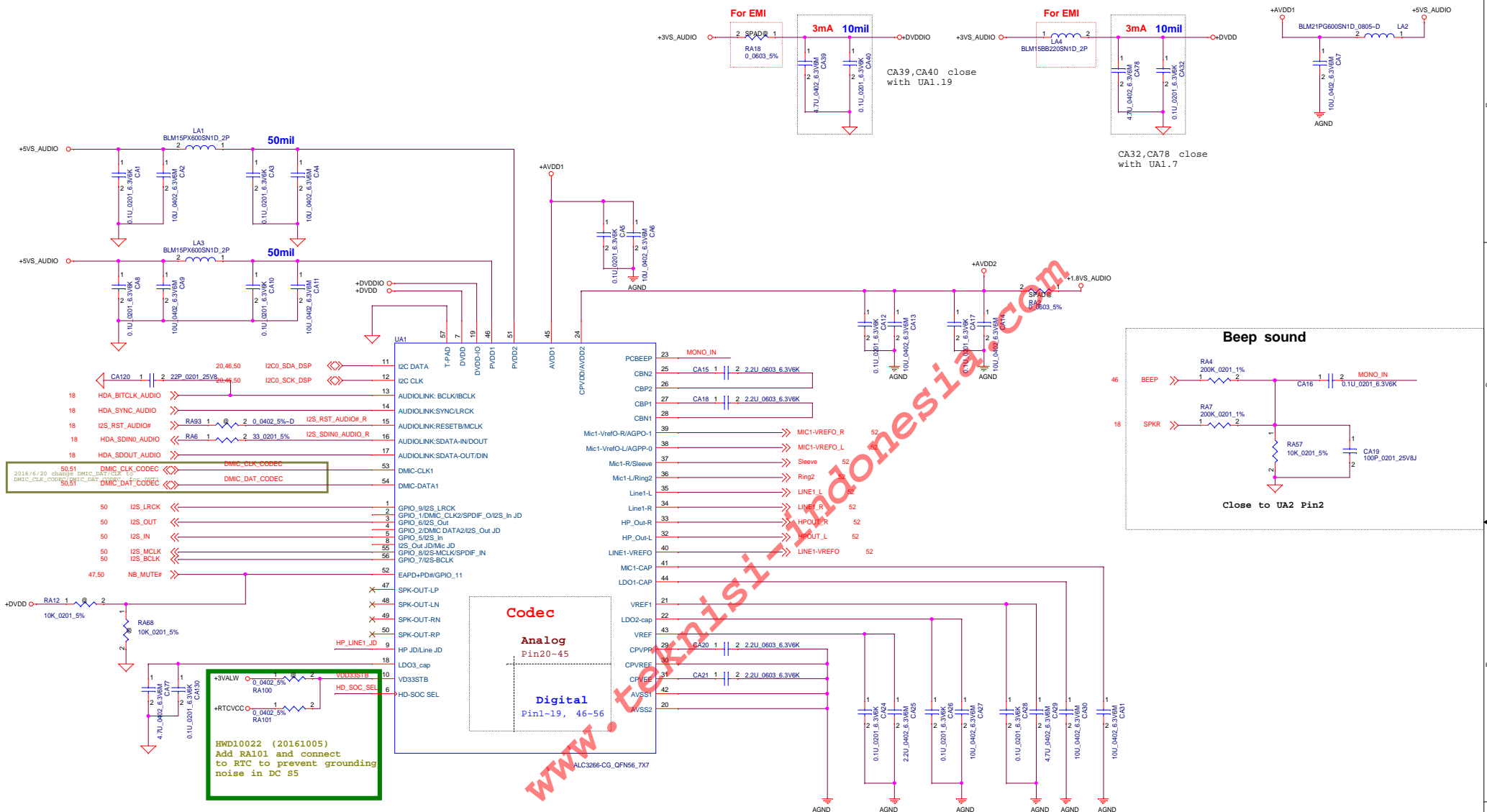


RTC Battery With Charge Function



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2011/08/25		2012/07/25		TPM/RTB conn.	
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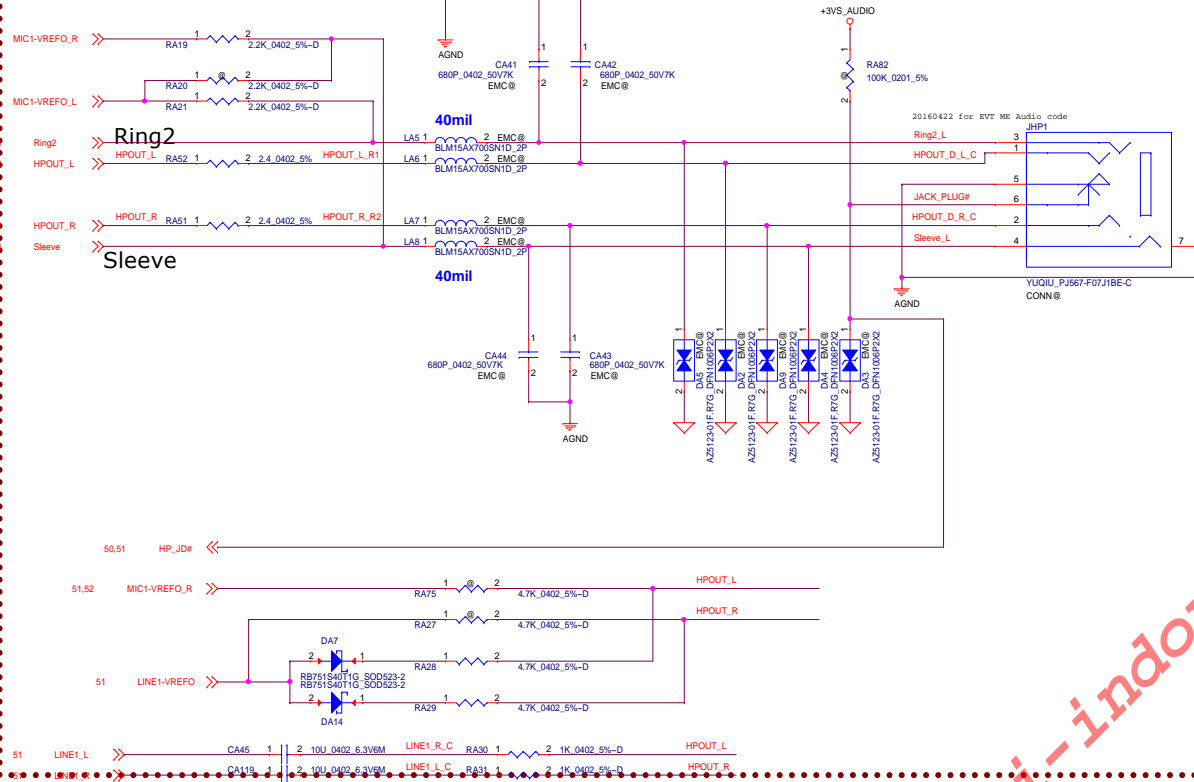
HD Audio Codec



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2013/07/04		2013/10/28		P21-Audio Codec	
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		Date: Wednesday, October 26, 2016		Sheet 51 of 75	

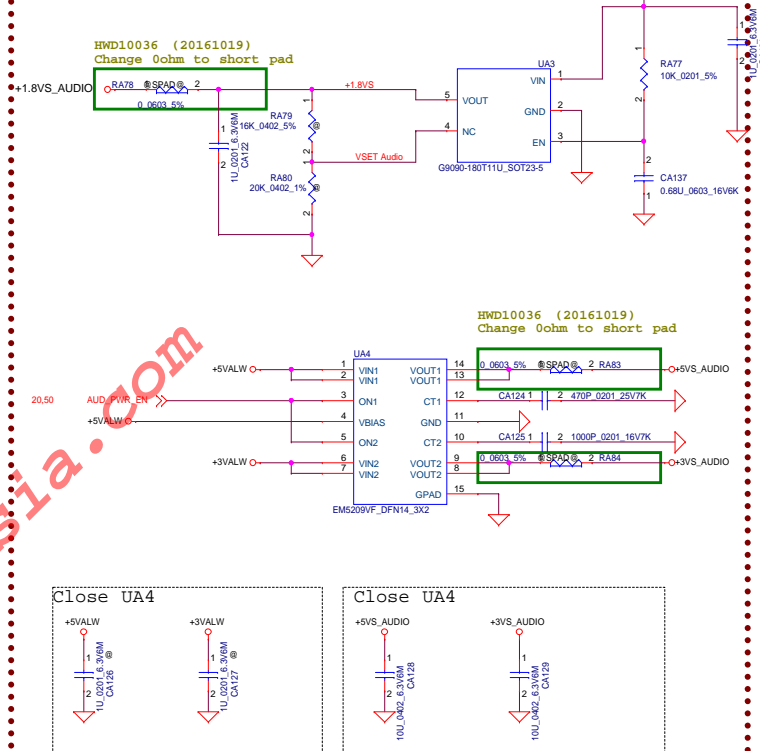
Universal Audio Jack

2016/03/27 follow Berlinetta Audio Jack circuit

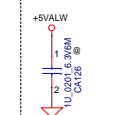


+3VS To +1.8VS_AUDIO

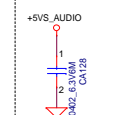
2016/03/27 follow Berlinetta +3VS To +1.8VS_AUDIO circuit



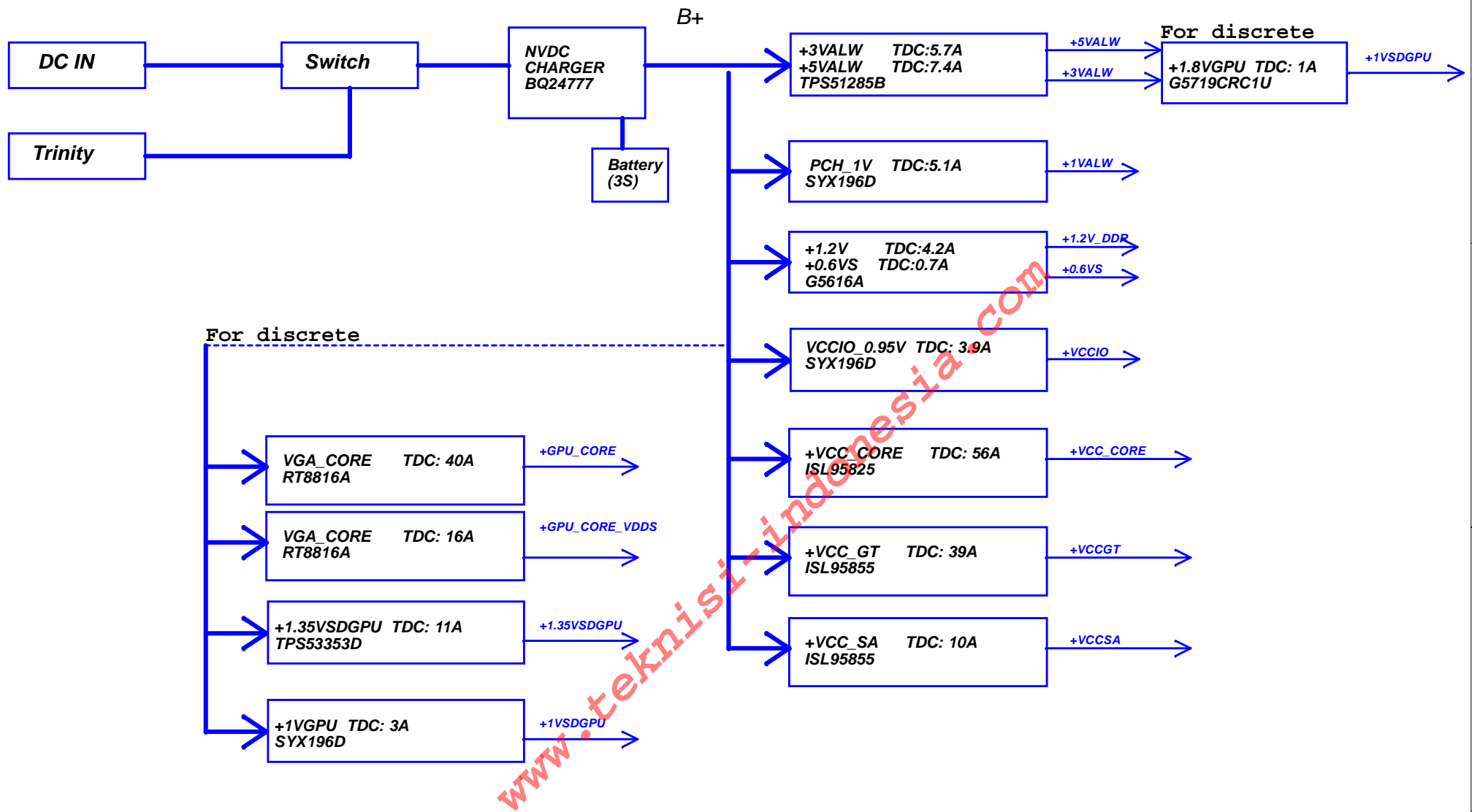
Close UA4

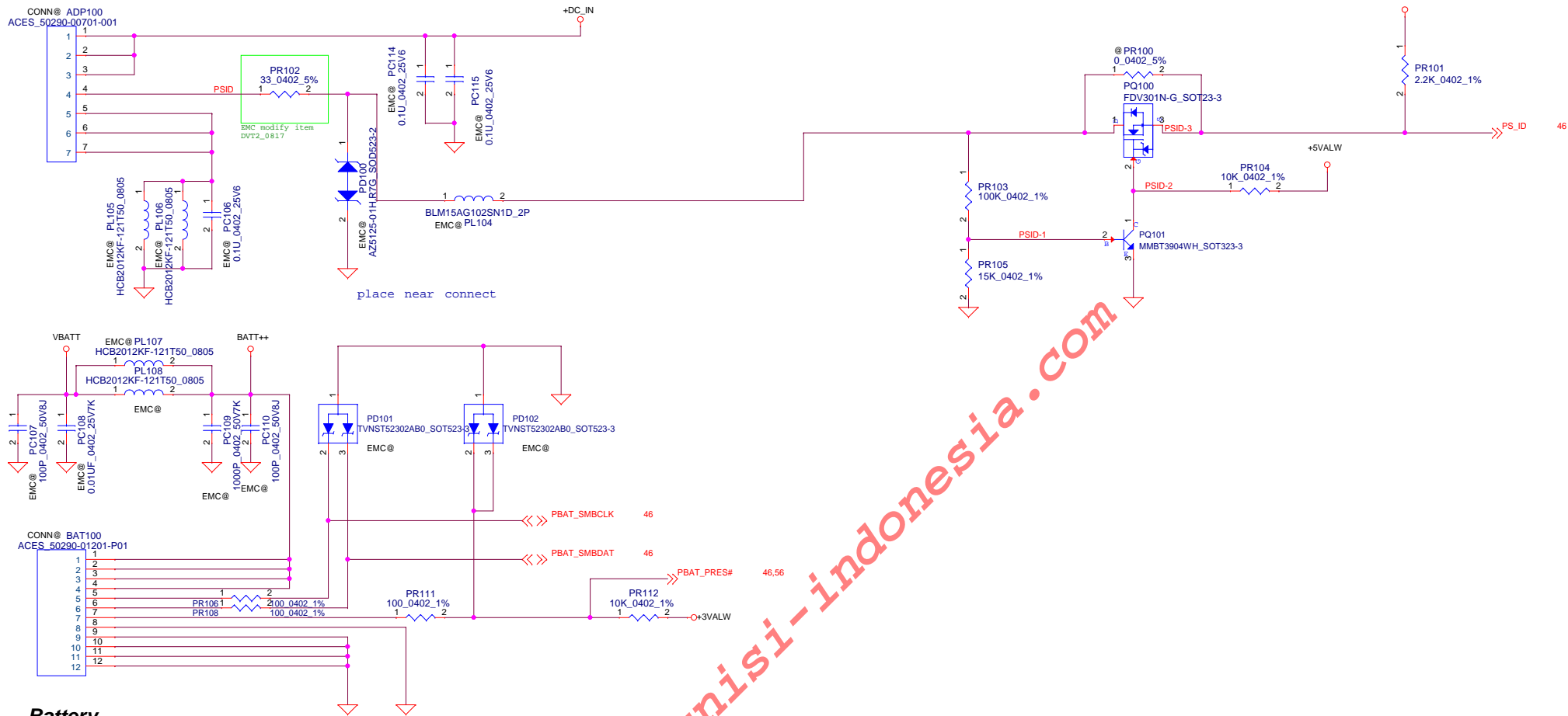


Close UA4



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**Battery
(3S3P)**

JIMBTY battery connector

SMART
Battery:
01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

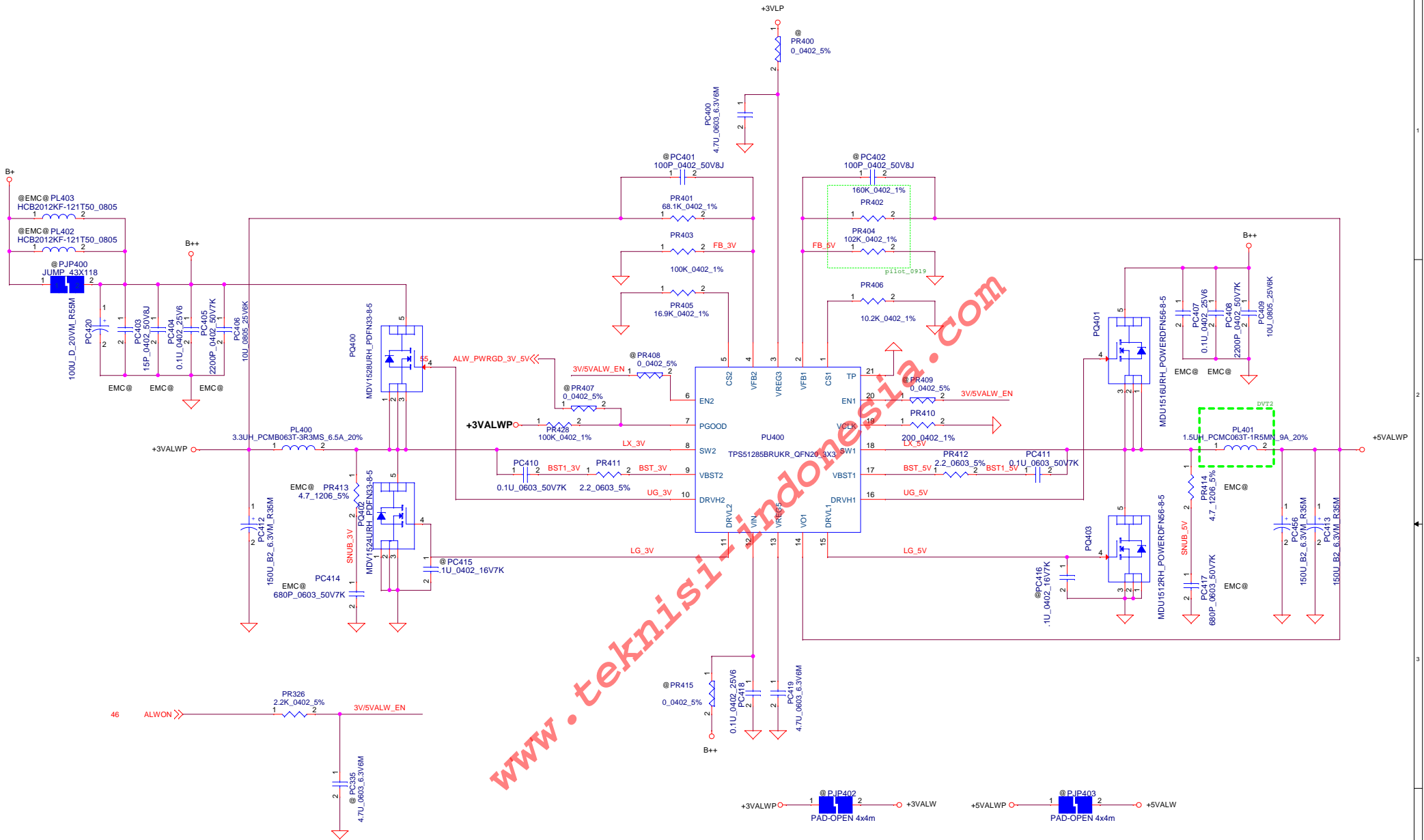
Smart Adapter circuit (39.1)

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Compal Electronics, Inc.

Title		
PWR-DCIN / BATT CONN / OTP		
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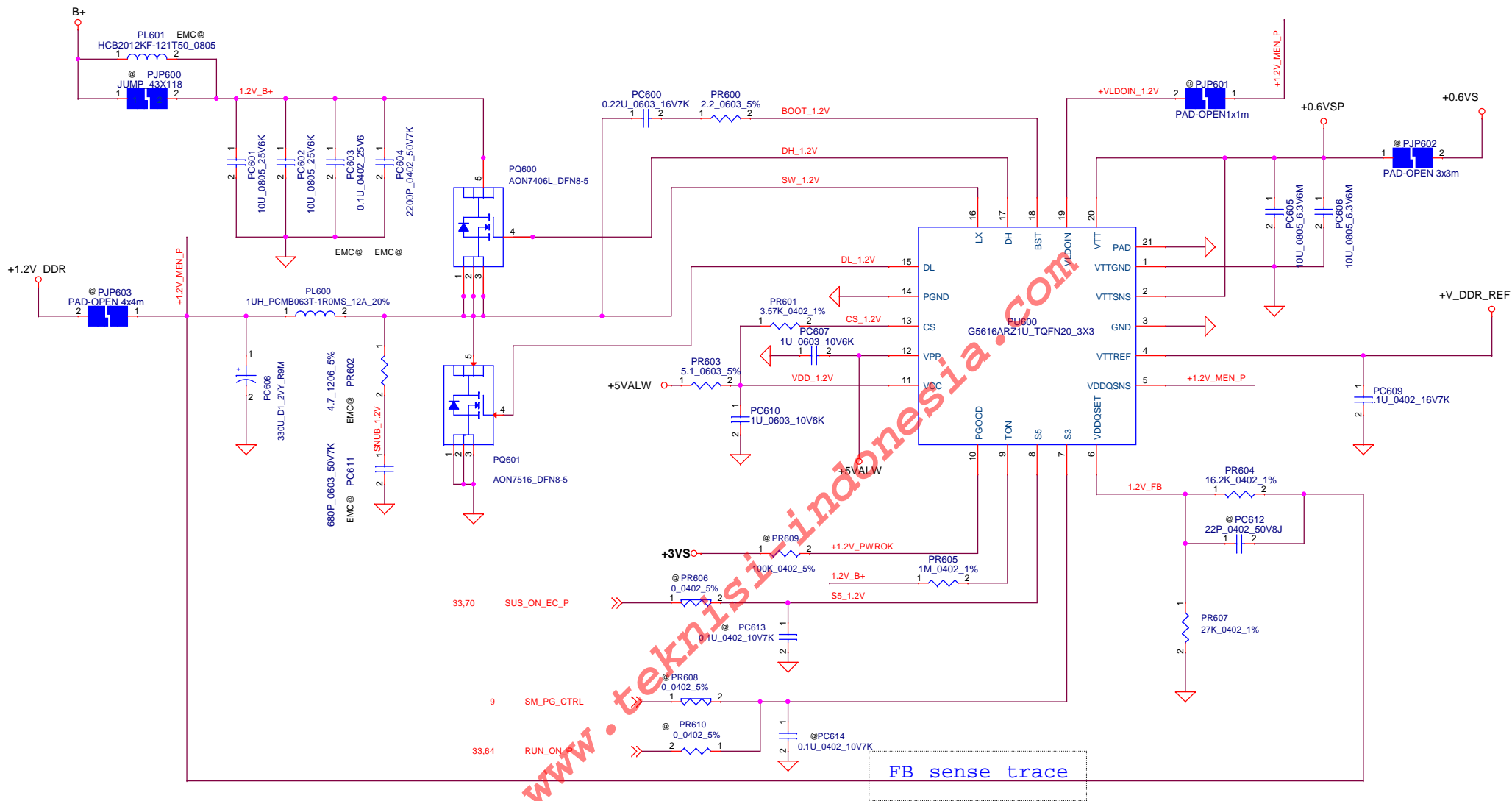
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3.3VALWP
TDC 5.7A
Peak Current 8.1A
OCP current 9.7A

5VALWP
TDC 7.4A
Peak Current 10.5A
OCP current 12.6A

3V/5V controller(35.1), Support component(35.2)

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1.2Volt +/- 5%
TDC 4.2A
Peak Current 6A
OCP current 7.2A

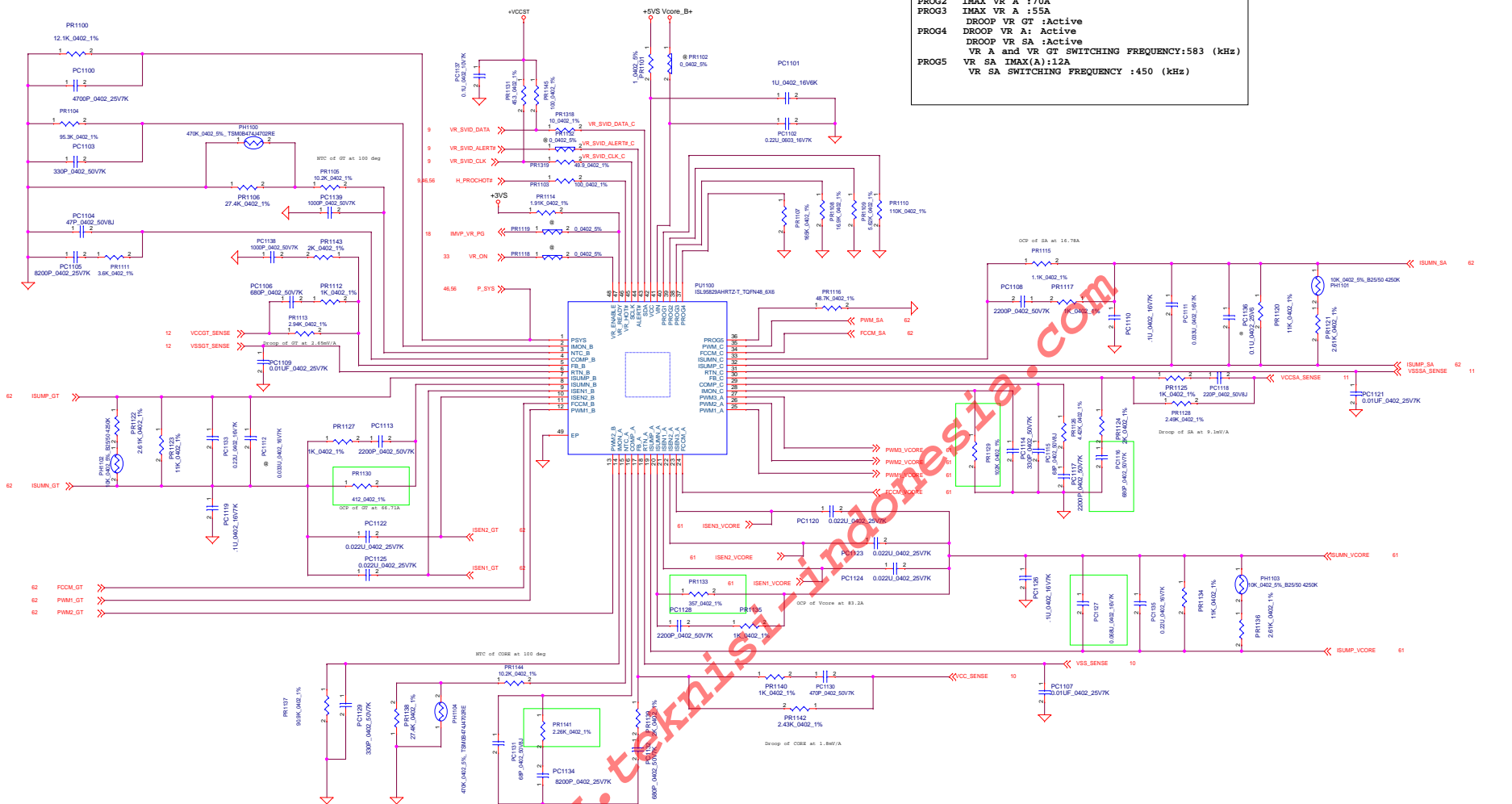
0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

DDR controller(35.3), Support component(35.4)

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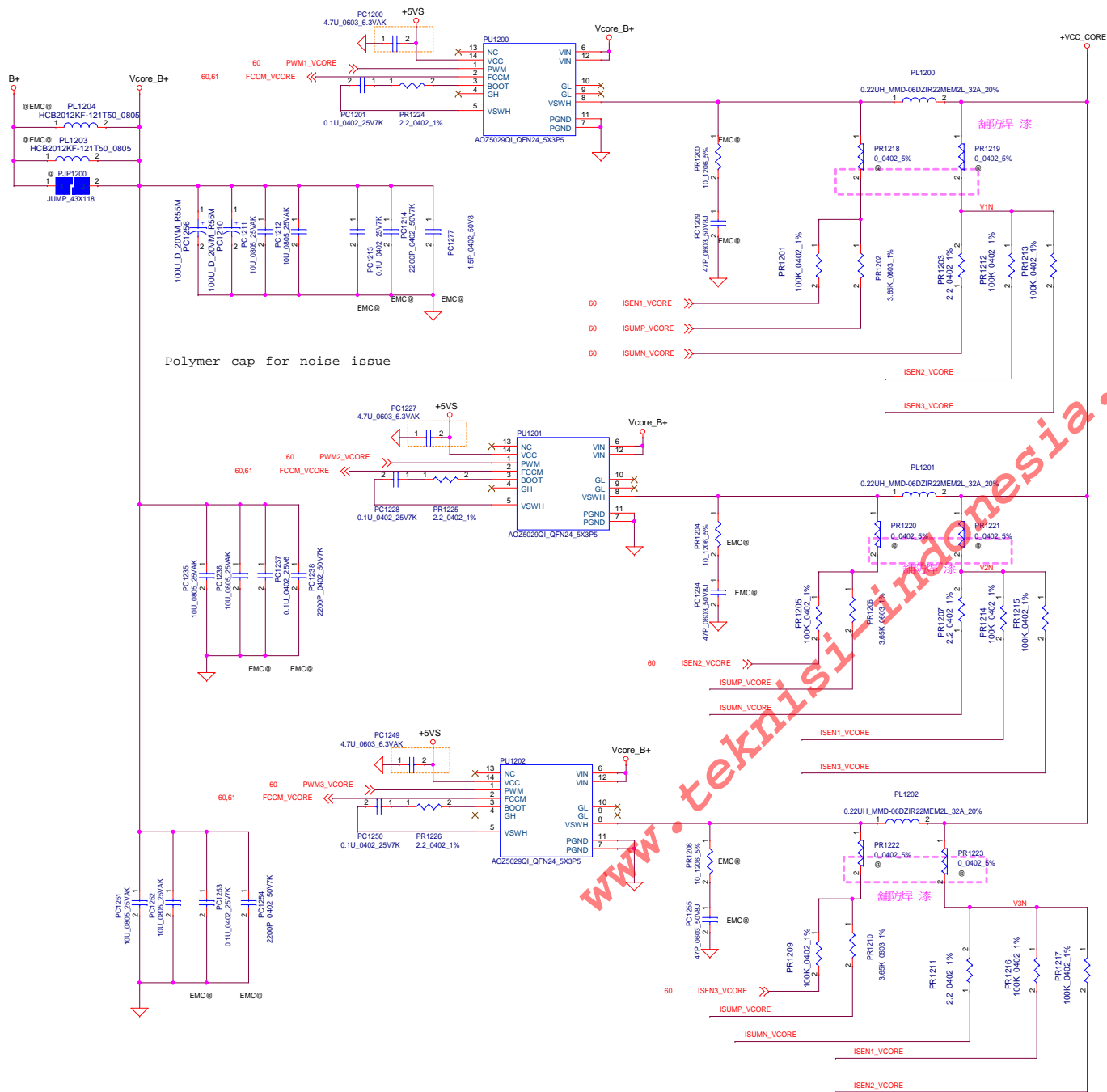
Compal Electronics, Inc.			
Title			
+1.35V_MEN/+0.675V_DDR_VTT			
Size			
Document Number			
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Date: Wednesday, October 26, 2016			
Sheet 59 of 75			
Rev 0.1(000)			

PROG sets
 PROG1 Vboot :0V
 slew rate :30 mV/uS
 PROG2 IMAX VR A :70A
 PROG3 IMAX VR A :55A
 PROG4 DROOP VR GT :Active
 DROOP VR A: Active
 DROOP VR SA :Active
 PROG5 VR A and VR GT SWITCHING FREQUENCY:583 (kHz)
 VR SA IMAX(A):12A
 VR SA SWITCHING FREQUENCY :450 (kHz)



CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3)
 Acoustic Noise B+ Bdk CAR 37.2

File	<Title>
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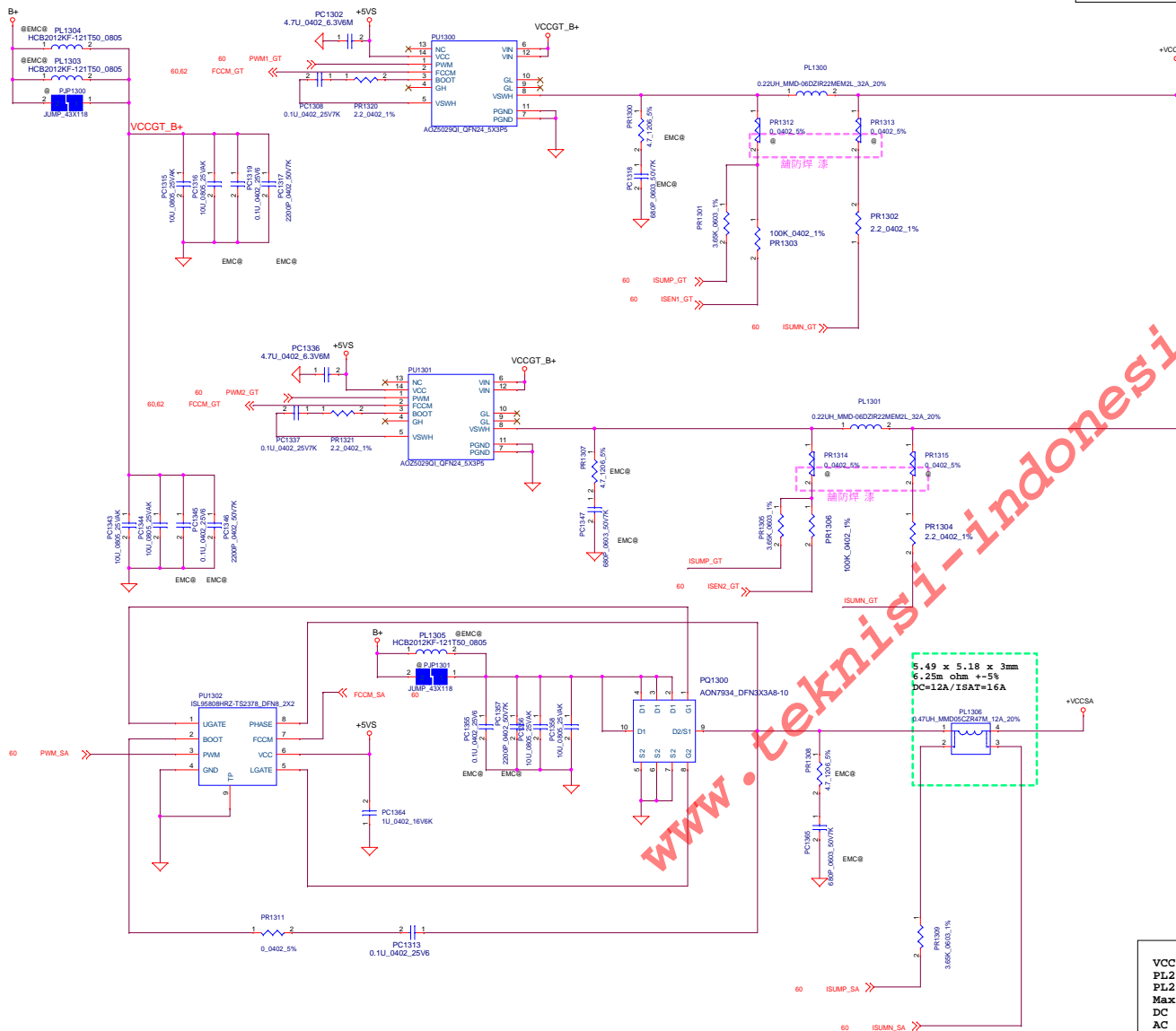


VCC_core
 PL2 TDC_default):50A
 PL2 TDC_max (40Sec):56A
 Peak Current 68A
 DC Load line -1.8mV/A
 AC Load line -1.8mV/A
 OCP Current 83.2A
 DCR 0.97mohm +/-5%

CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3)
 CPU_Core output CAP(36.4), Acoust i c Nöse B+ Bük AR 37.2

Title		<Title>	Rev 0.1(000)
Size	Document Number	LA-E331P	
Date:	Wednesday, October 26, 2016	Sheet	61 of 75

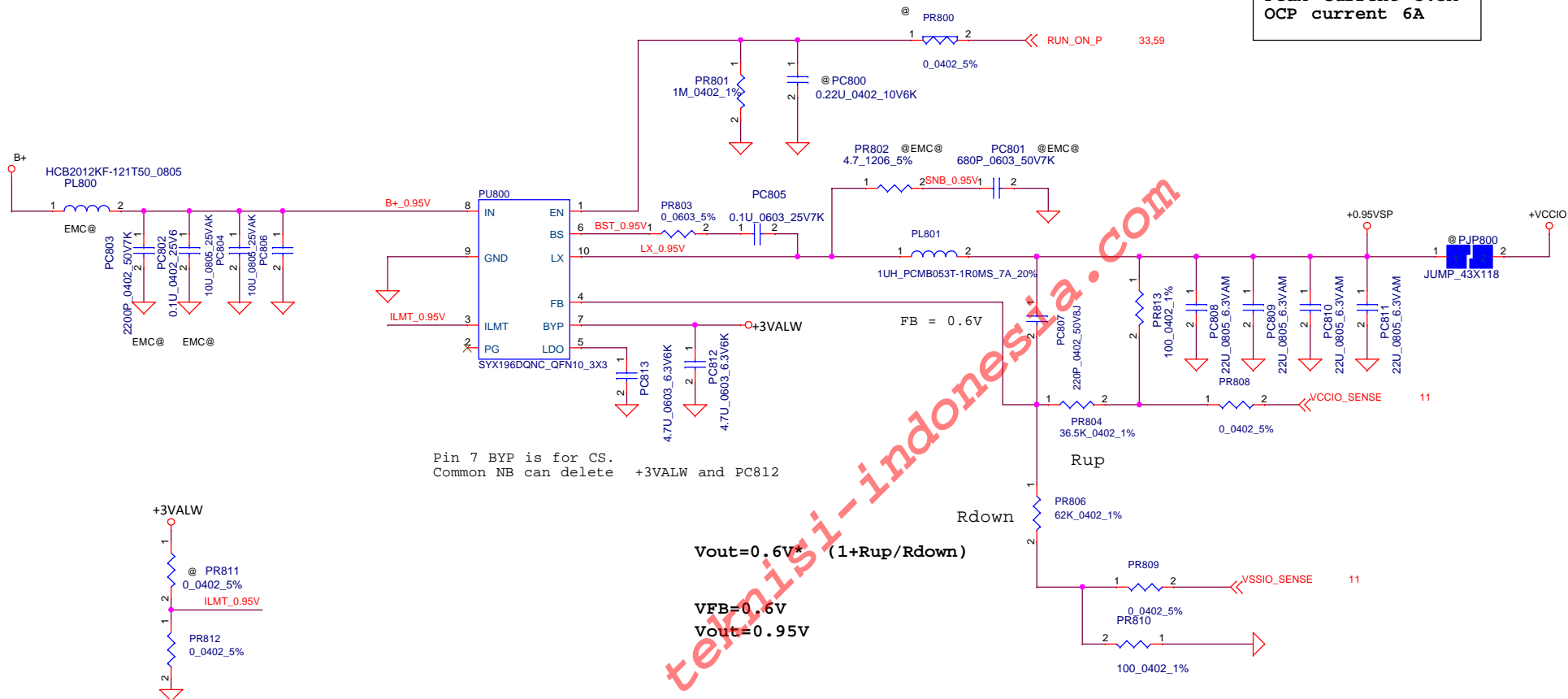

```
VCCGT (Base on PDDG rev 0.7)
PL2 TDC_default):25
PL2 TDC_max (40Sec):39A
Max Current 55A
DC Load line -2.65mV/A
AC Load line -2.65mV/A
OCP Current 66.7A
DCR 0.98mohm +/-5%
```



```
VCCSA (Base on PDDG rev 0.7)
PL2 TDC_default):10A
PL2 TDC_max (40Sec):10A
Max Current 11A
DC Load line -9.1mV/A
AC Load line -9.1mV/A
OCP Current 20A
DCR 6.2 ± 5%
```

CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3), GFX output CAP(36.5)

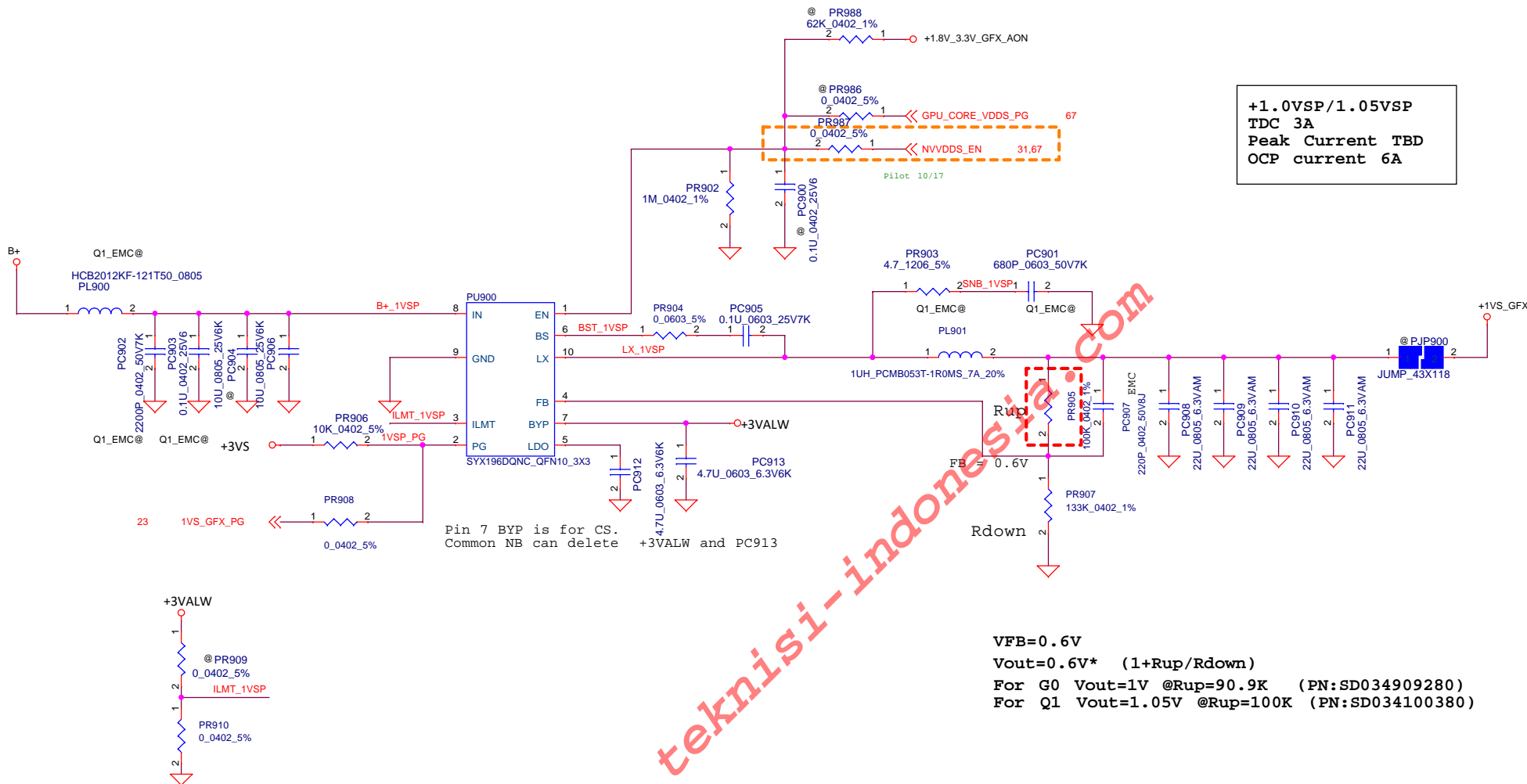
Title				<Title>			
Size	Document Number						Rev
Custom	LA-E331P						0.1(P00)
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The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

1.05V controller(35.5), Support component(35.6)

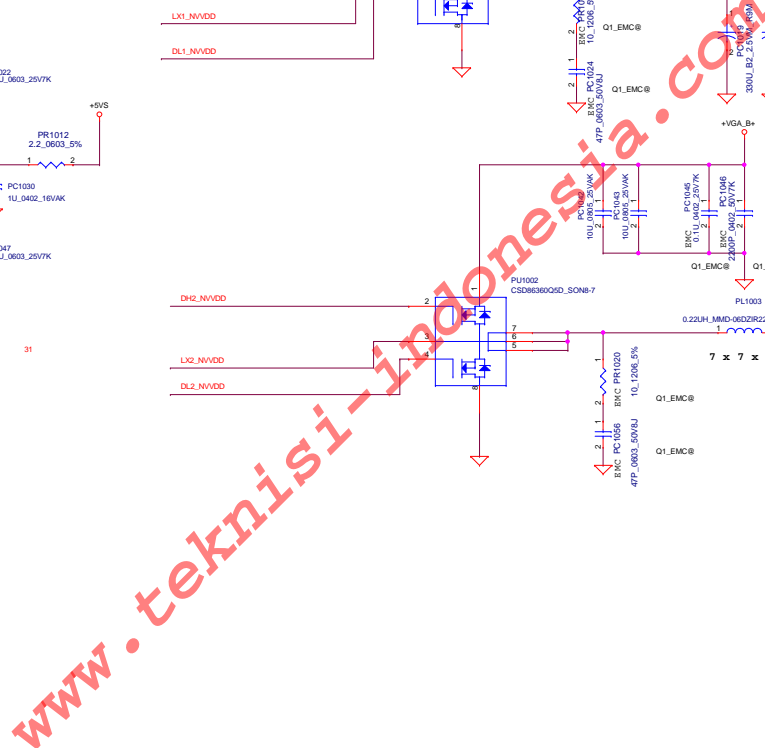
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P67-PWR +0.95VA
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	2Phase DEM	2Phase CCM
PSI	1.2V	1.8V
Rb	22.6Kohm	0ohm
Rc	169Kohm	NC

		MIN		MAX
H/S	Rds(on)	:	3.7mohm	, 4.5mohm
L/S	Rds(on)	:	1.5mohm	, 1.9mohm



Near:
10U_0805_6.3V6M*7
22U_0805_6.3V6M *7
4.7U_0805_6.3V6K *6
330u*3

- VGA_CORE controller(43.1), Support component(43.2)
- VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

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VGA_CORE

ent Number
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Page No.	Date	Topic	Page No.	Date	Topic
1	10/10/2020	Introduction to the course	2	11/10/2020	Mathematical Preliminaries
3	12/10/2020	Linear Algebra	4	13/10/2020	Calculus
5	14/10/2020	Probability	6	15/10/2020	Statistics
7	16/10/2020	Optimization	8	17/10/2020	Game Theory
9	18/10/2020	Decision Making	10	19/10/2020	Conclusion

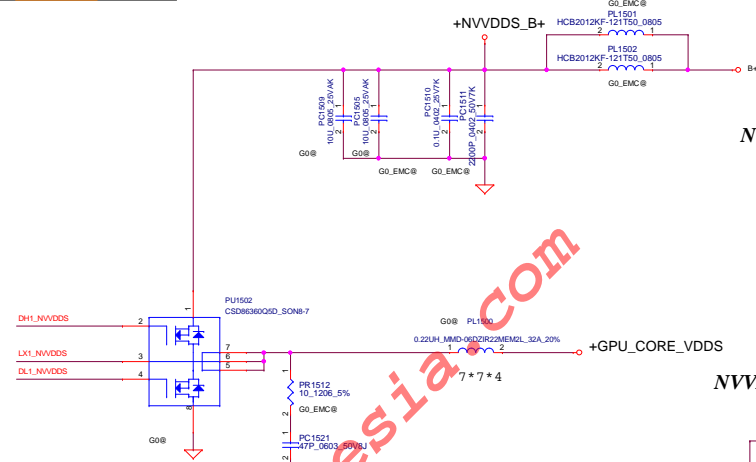
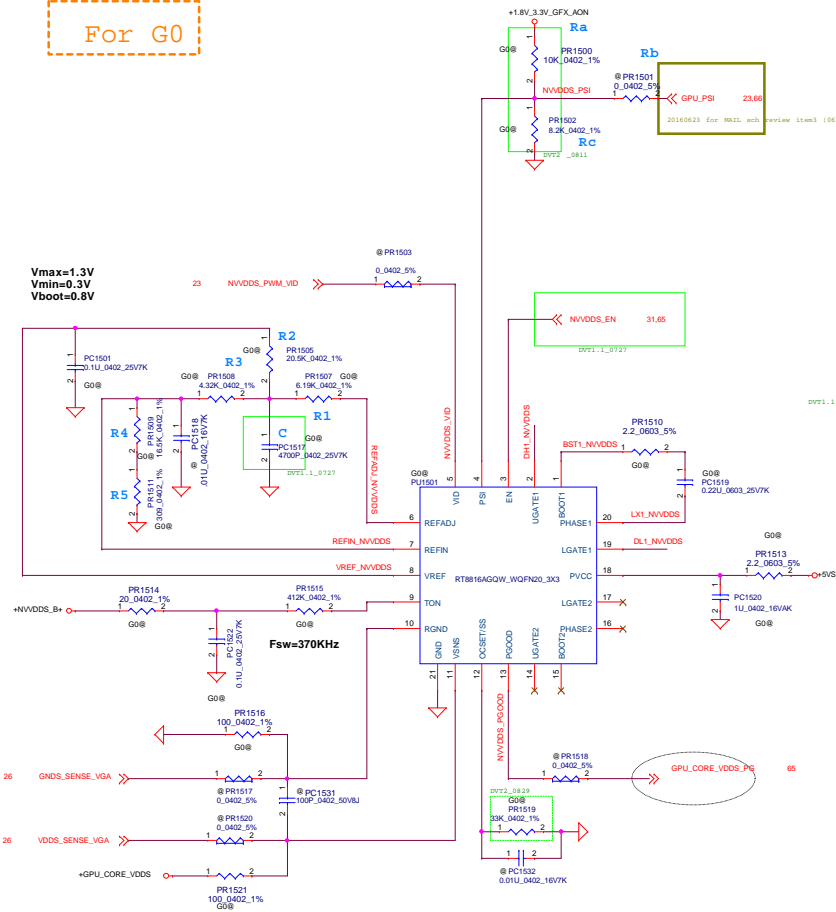
For G0

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V

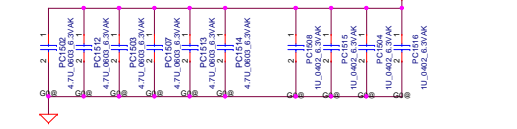
	1phase DEM	1phase CCM
PS1	0V	
Ra	NC	10Kohm
Rb	NC	0ohm
Rc	0ohm	8.06kohm

+GPU_CORE_VDD5
TDC 12A
Peak Current 16A
OCP current 21A
DCR 0.98mohm +/- 5%

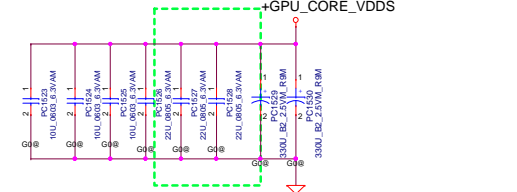
H/S Rds(on) : 3.7mohm , 4.5mohm
L/S Rds(on) : 1.5mohm , 1.9mohm



NVVDD5 (place under GPU)



NVVDD5 (place near GPU)



Under:
4.7U_0603_6.3VAK *6
1U_0402_6.3VAK *4

Near:
10U_0603_6.3V6M *3
22U_0805_6.3V6M *3
330u*2

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

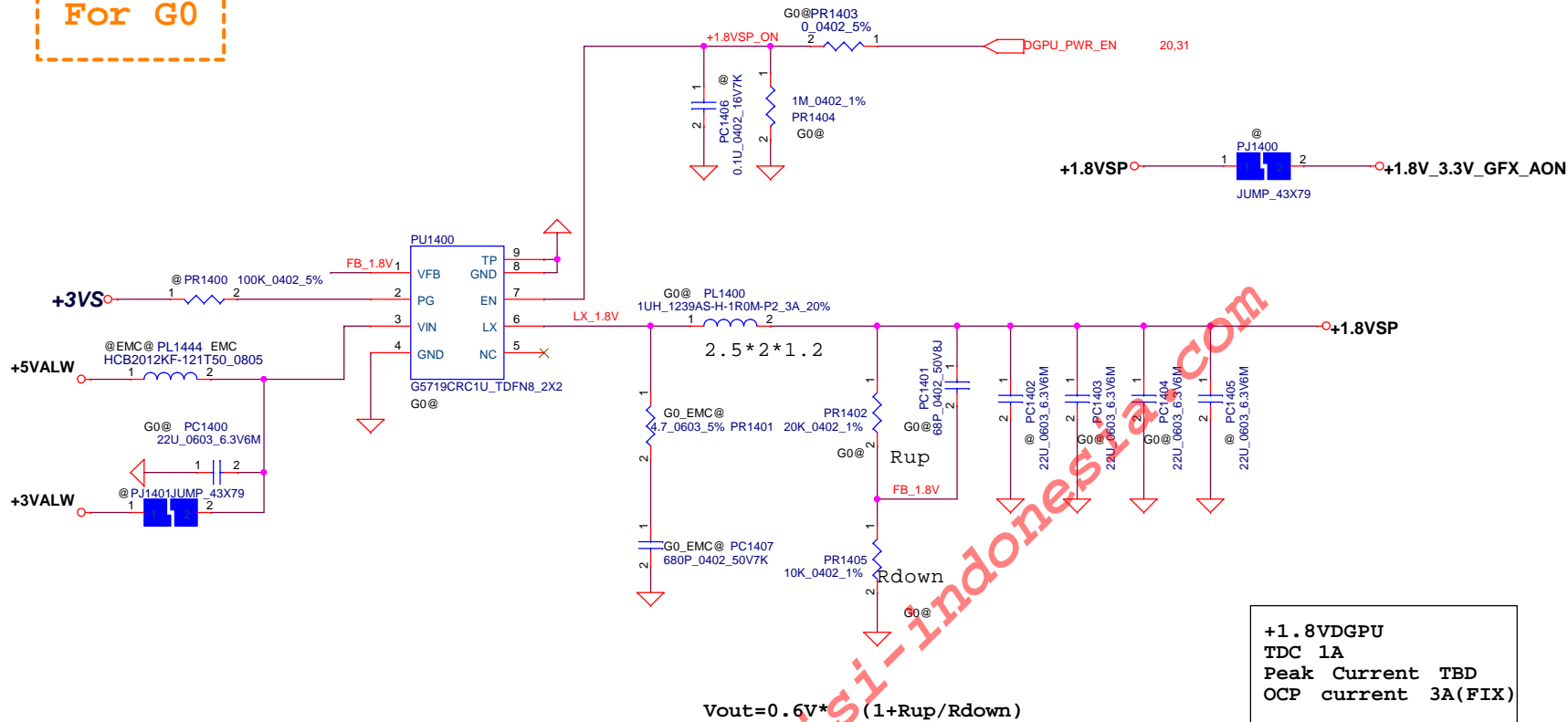
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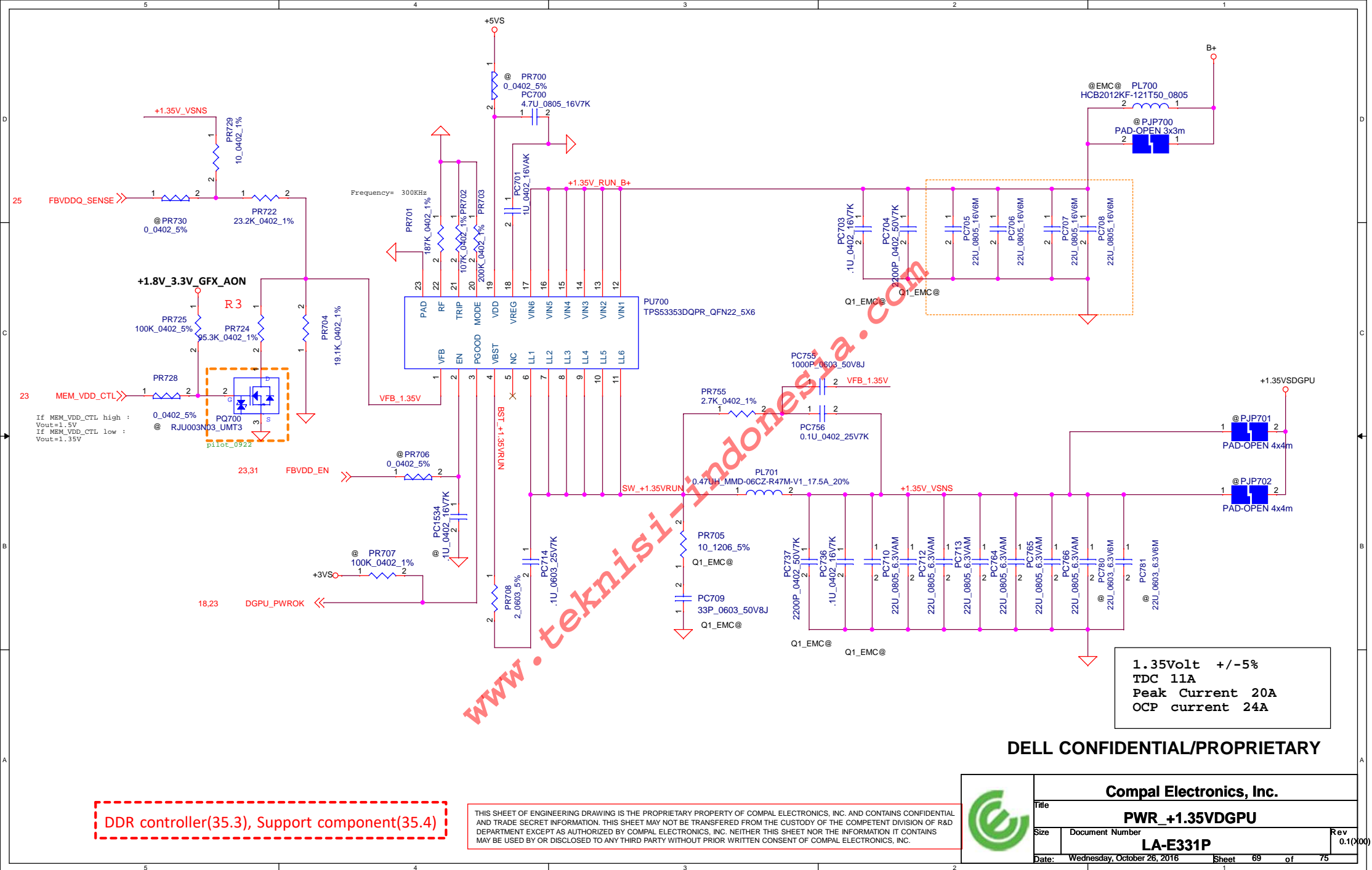
Compal Electronics, Inc.			
File	+GPU_CORE_VDD5		
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For G0



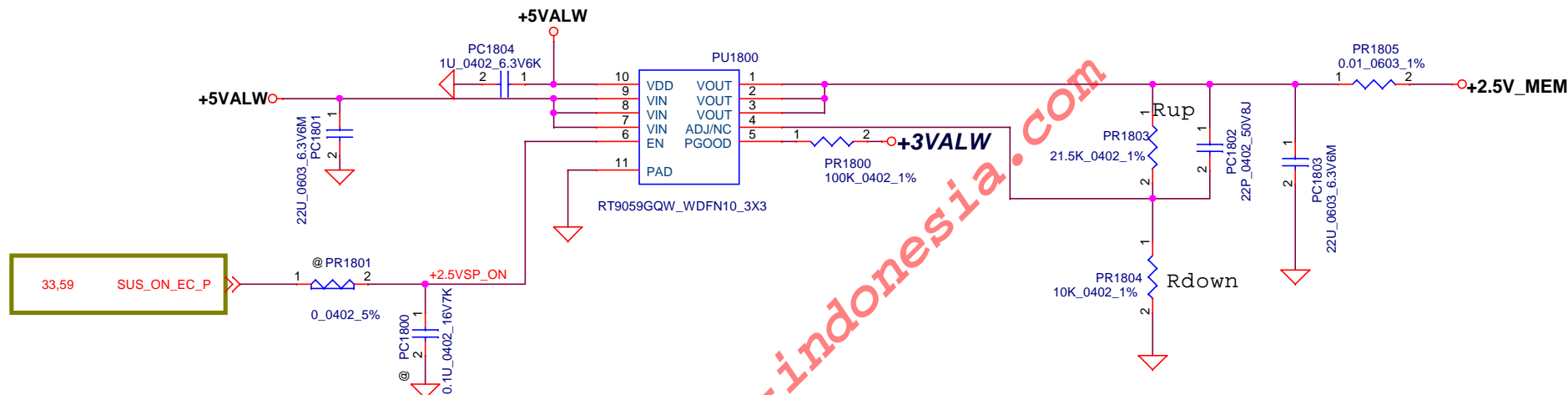
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2.5V_MEM controller(35.13), Support component(35.14)

+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A

EE no need 2.5V_PWROK
Delete 2.5V_PWROK



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